CDP1854A, CDP1854AC

Programmable Universal Asynchronous Receiver/Transmitter (UART)

March 1997

Features

- **Two Operating Modes**
  - **Mode 0 - Functionally Compatible with Industry Types Such as the TR1602A and CDP6402**
  - **Mode 1 - Interfaces Directly with CDP1800-Series Microprocessors without Additional Components**
- **Full or Half Duplex Operation**
- **Parity, Framing and Overrun Error Detection**
- **Baud Rate**
  - **DC to 200K Bits/s at V_{DD} 5V**
  - **DC to 400K Bits/s at V_{DD} 10V**
- **Fully Programmable with Externally Selectable Word Length (5-8 Bits), Parity Inhibit, Even/Odd Parity, and 1, 1-1/2, or 2 Stop Bits**
- **False Start Bit Detection**

Ordering Information

PACKAGE	TEMP. RANGE	5V/200K BAUD	10V/400K BAUD	PKG. NO.
PDIP	-40°C to +85°C	CDP1854ACE	CDP1854AE	E40.6
Burn-In		CDP1854ACEX	CDP1854AEX	E40.6
PLCC	-40°C to +85°C	CDP1854ACQ	CDP1854AQ	N44.65
SBDIP	-40°C to +85°C	CDP1854ACD	CDP1854AD	D40.6
Burn-In		CDP1854ACDX	-	D40.6

Description

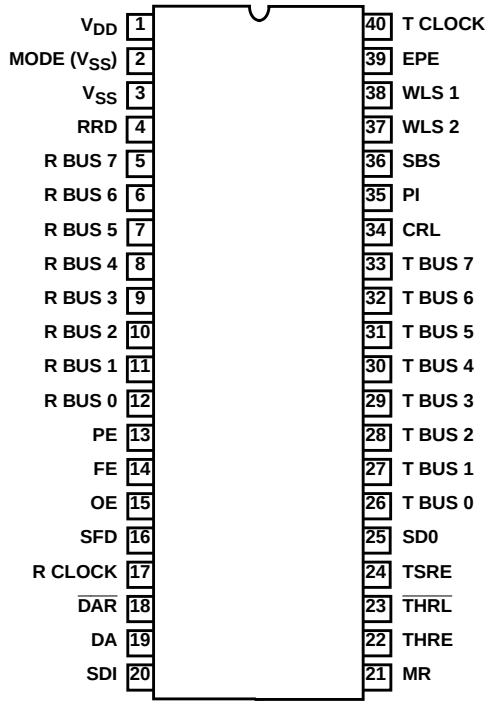
The CDP1854A and CDP1854AC are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854A UART can be programmed to operate in one of two modes by using the mode control input. When the input is high (MODE = 1), the CDP1854A is directly compatible with the CDP1800-series microprocessor system without additional interface circuitry. When the mode input is low (MODE = 0), the device is functionally compatible with industry standard UART's such as the TR1602A and CDP6402. It is also pin compatible with these types, except that pin 2 is used for the mode control input.

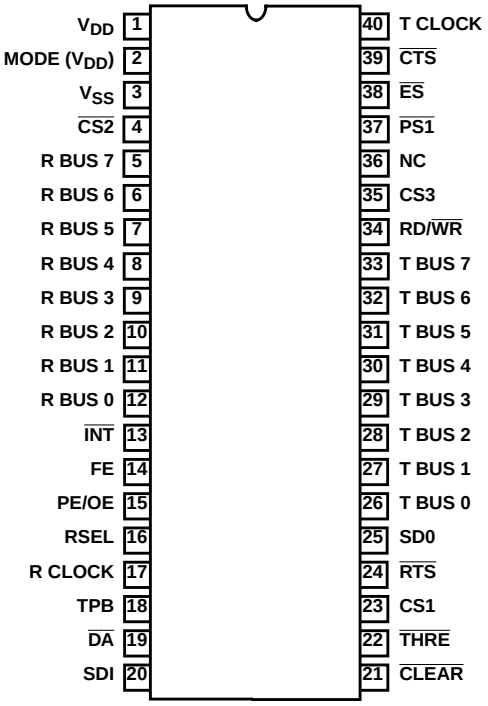
The CDP1854A and the CDP1854AC are functionally identical. The CDP1854A has a recommended operating voltage range of 4V to 10.5V, and the CDP1854AC has a recommended operating voltage range of 4V to 6.5V.

Pinouts

40 LEAD SBDIP, PDIP (MODE 0)
TOP VIEW

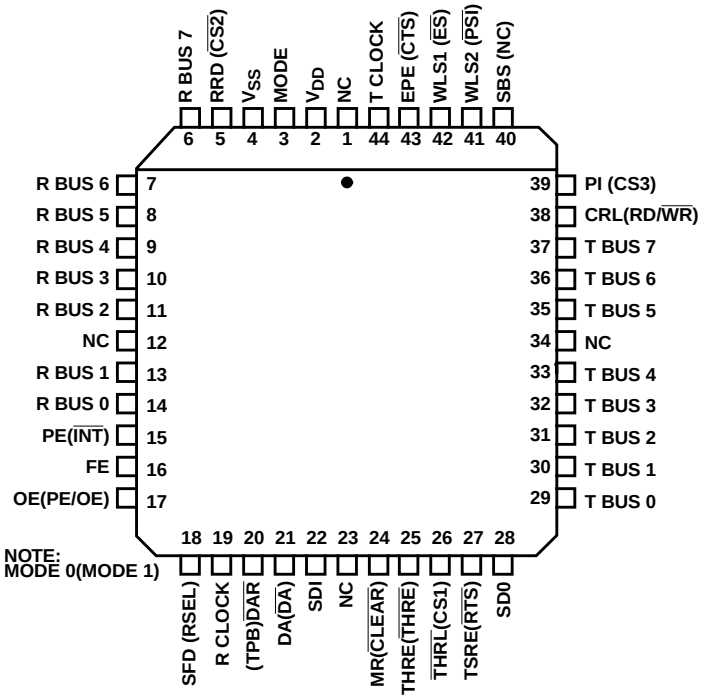


40 LEAD SBDIP, PDIP (MODE 1)
TOP VIEW



NC = NO CONNECT

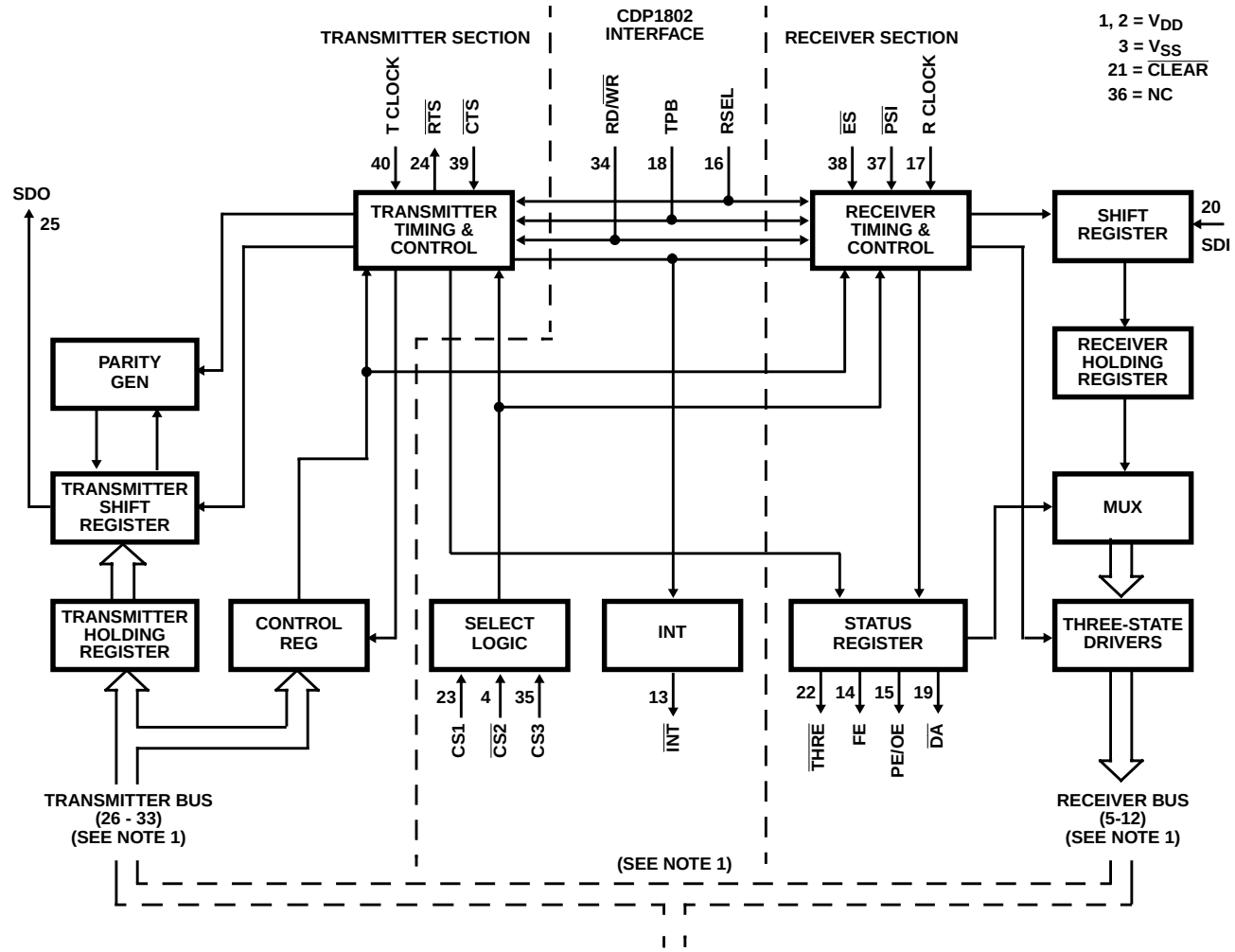
44 LEAD PLCC (Q SUFFIX)
TOP VIEW



NOTE:
MODE 0(MODE 1)

Block Diagram

Mode Input High (Mode = 1)



NOTE: 1. User Interconnect

FIGURE 1. MODE 1 BLOCK DIAGRAM (CDP1800-SERIES MICROPROCESSOR COMPATIBLE)

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(Voltages Referenced to V_{SS} Terminal)
CDP1854A . . . . . -0.5 to +11V
CDP1854AC . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} + 0.5V
DC Input Current, Any One Input. . . . . ±10mA
Device Dissipation Per Output Transistor
T_A = Full Package-Temperature Range 100mW
Operating-Temperature Range (T_A)
Package Type D . . . . . -55^oC to $+125^oC$
Package Type E and Q . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	55	15
PDIP Package	50	N/A
PLCC Package	46	N/A

Maximum Junction Temperature
Plastic Package . . . . . $+150^oC$
Ceramic Package . . . . . $+175^oC$
Maximum Storage Temperature Range (T_{STG}) . . . -65^oC to $+150^oC$
Maximum Lead Temperature (Soldering 10s):
At Distance 1/16 ±1/32 inch (1.59 ±0.79mm) . . . . . $+265^oC$
NOTE: Printed circuit board mount: 57mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications at $T_A = -40^oC$ to $+85^oC$, Unless Otherwise Noted

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1854A MIN	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A MAX	LIMITS CDP1854AC MIN	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current (Except pins 24 and 25)	I_{OL}	0.4	0, 5	5	1	2	-	1	2	-	mA
		0.5	0, 10	10	2	4	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.55	-1.1	-	-0.55	-1.1	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	-	-	-	mA
Output Low Drive (Sink) Current (Pins 24 and 25)	I_{OL}	0.4	0, 5	5	1.6	3.5	-	1.6	3.5	-	mA
		0.5	0, 10	10	3.2	7	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Current	I_{IN}	-	0, 5	5	-	-	±1	-	-	±1	µA
		-	0, 10	10	-	-	±2	-	-	-	µA

Static Electrical Specifications at T_A = -40°C to +85°C, Unless Otherwise Noted **(Continued)**

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1854A			CDP1854AC			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±10	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	-	-	1.5	-	mA
		-	0, 10	10	-	6	-	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = 25°C.
2. $I_{OL} = I_{OH}$ = 1µA.
3. Operating current is measured at 200kHz or V_{DD} = 5V and 400kHz for V_{DD} = 10V in a CDP1800-series microprocessor system, with open outputs.

Operating Conditions At T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CONDITIONS	LIMITS				UNITS
		CDP1854A		CDP1854AC		
	V_{DD} (V)	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	-	4	10.5	4	6.5	V
Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Baud Rate (Receive or Transmit)	5	-	200	-	200	K bits/s
	10	-	400	-	-	K bits/s

Functional Definitions for CDP1854A Terminals Mode 1 CDP1800-Series Microprocessor Compatible

SIGNAL: FUNCTION

V_{DD}:

Positive supply voltage.

MODE SELECT (MODE):

A high-level voltage at this input selects CDP1800-series microprocessor Mode operation.

V_{SS}:

Ground

$\overline{\text{CHIP SELECT 2}}$ ($\overline{\text{CS2}}$):

A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

$\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$):

A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table 1.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):

A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Table 2).

REGISTER SELECT (RSEL):

This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table 3.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

TPB:

A positive input pulse used as a data load or reset strobe.

$\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$):

A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

$\overline{\text{CLEAR}}$ ($\overline{\text{CLEAR}}$):

A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

$\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$):

A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):

A high-level voltage at this input together with $\overline{\text{CS2}}$ and CS3 selects the UART.

$\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$):

This output signal tells the peripheral to get ready to receive data. $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) is the response from the peripheral. $\overline{\text{RTS}}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register [start bit, data bits, parity bit, and stop bit(s)] are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/$\overline{\text{WR}}$:

A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):

With high-level voltage at this input together with CS1 and $\overline{\text{CS2}}$ selects the UART.

$\overline{\text{PERIPHERAL STATUS INTERRUPT}}$ ($\overline{\text{PSI}}$):

A high-to-low transition on this input line sets a bit in the Status Register and causes an $\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$ = low).

$\overline{\text{EXTERNAL STATUS}}$ ($\overline{\text{ES}}$):

A low-level voltage at this input sets a bit in the Status Register.

CLEAR TO SEND ($\overline{CTS}$):

When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

TABLE 1. INTERRUPT SET AND RESET CONDITIONS

(NOTE 1) SET (INT = LOW)	RESET (INT = HIGH)	
CAUSE	**CONDITION**	**TIME**
DA (Receipt of Data)	Read of Data	TPB Leading Edge
THRE (Note 2) (Ability to Reload)	Read of Status or Write of Character	TPB Leading Edge
THRE • TSRE (Transmitter Done)	Read of Status or Write of Character	TPB Leading Edge
$\overline{PSI}$ (Negative Edge)	Read of Status	TPB Trailing Edge
$\overline{CTS}$ (Positive Edge when $\overline{THRE} \bullet \overline{TSRE}$)	Read of Status	TPB Leading Edge

NOTES:

1. Interrupts will occur only after the IE bit in the Control Register (see Table 4) has been set.
2. THRE will cause an interrupt only after the TR bit in the Control Register (see Table 4) has been set.

TABLE 2. STATUS REGISTER BIT ASSIGNMENT

BIT	7	6	5	4	3	2	1	0
SIGNAL	THRE	TSRE	PSI	ES	FE	PE	OE	DA
ALSO AVAILABLE AT TERMINAL † Polarity reversed at output terminal.	22†	-	-	-	14	15	15	19†

BIT SIGNAL: FUNCTION	
0	DATA AVAILABLE (DA): When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.
1	OVERRUN ERROR (OE): When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.
2	PARITY ERROR (PE): When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.
3	FRAMING ERROR (FE): When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.
4	EXTERNAL STATUS (ES): This bit is set high by a low-level input at Term. 38 ($\overline{ES}$).
5	PERIPHERAL STATUS INTERRUPT (PSI): This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{PSI}$). The INTERRUPT output (Term. 13) is also asserted ($\overline{INT}$ = low) when this bit is set.
6	TRANSMITTER SHIFT REGISTER EMPTY (TSRE): When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.
7	TRANSMITTER HOLDING REGISTER EMPTY (THRE): When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{THRE}$ output (Term. 22) low and causes an INTERRUPT ($\overline{INT}$ = low), if TR is high.

Description of Mode 1 Operation CDP1800-Series Microprocessor Compatible (Mode Input = V_{DD})

Initialization and Controls

In the CDP1800-series microprocessor compatible mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/$\overline{WR}$ and RSEL inputs as follows:

TABLE 3. REGISTER SELECTION SUMMARY

RSEL	RD/$\overline{WR}$	FUNCTION
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1800-series microprocessor I/O control output signals can be connected directly to the CDP1854A inputs as shown in Figure 2. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1• $\overline{CS2}$ • CS3 = 1) and the Control Register is designated (RSEL = H, RD/$\overline{WR}$ = L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0 - R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Table 2.

Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Table 4) is set. Loading the Control Register with TR = 1 (bit 7 = high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a $\overline{TRANSMITTER\ HOLDING\ REGISTER\ EMPTY}$ ($\overline{THRE}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND ($\overline{RTS}$) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable $\overline{THRE}$ interrupts and to generate the $\overline{RTS}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 • $\overline{CS2}$ • CS3 = 1, and the Holding Register is selected by RSEL = L and RD/$\overline{WR}$ = L. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{CTS}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB and transmission of a start bit will occur 1/2 clock period later (see Figure 3). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE • TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Table 4). SDO is held low until the BREAK bit is reset.

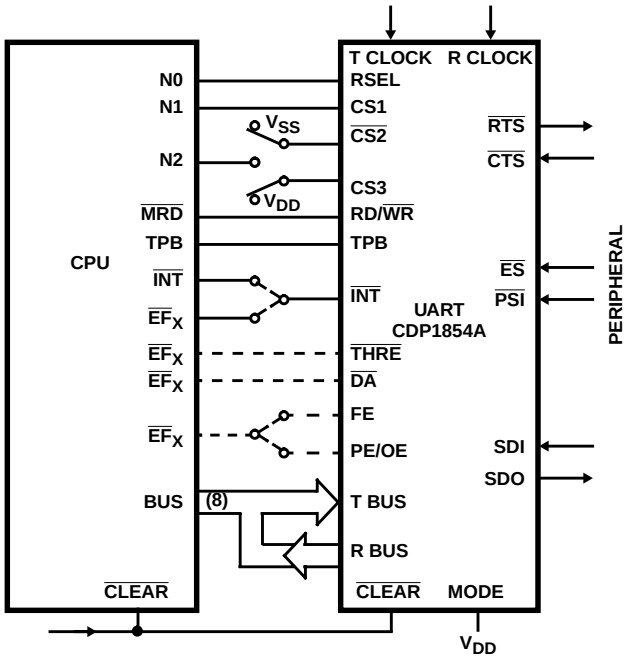


FIGURE 2. RECOMMENDED CDP1800-SERIES CONNECTION, MODE 1 (NON-INTERRUPT DRIVEN SYSTEM)

Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2

in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the DATA AVAILABLE (DA) and INTERRUPT (INT) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's three-state bus drivers are enabled when the UART is selected (CS1 • $\overline{CS2}$ • CS3 = 1) and RD/$\overline{WR}$ = high. Status can be read when RSEL = high. Data is read when RSEL = low. When reading data, TPB latches data in the microprocessor and resets $\overline{\text{DATA AVAILABLE}}$ ($\overline{DA}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The $\overline{\text{REQUEST TO SEND}}$ ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The $\overline{\text{CLEAR TO SEND}}$ ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The $\overline{\text{EXTERNAL STATUS}}$ ($\overline{ES}$) input latches a peripheral status level, and the $\overline{\text{PERIPHERAL STATUS INTERRUPT}}$ ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem $\overline{\text{DATA CARRIER DETECT}}$ line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Table 2).

TABLE 4. CONTROL REGISTER BIT ASSIGNMENT

BIT	7	6	5	4	3	2	1	0
SIGNAL	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

BIT SIGNAL: FUNCTION

0 PARITY INHIBIT (PI): When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1 EVEN PARITY ENABLE (EPE): When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2 STOP BIT SELECT (SBS): See table below.

3 WORD LENGTH SELECT 1 (WLS1): See table below.

4 WORD LENGTH SELECT 2 (WLS2): See table below.

5 INTERRUPT ENABLE (IE): When set high $\overline{THRE}$, DA, THRE • TSRE, $\overline{CTS}$, and PSI interrupts are enabled (see Interrupt Conditions, Table 1).

6 TRANSMIT BREAK (BREAK): Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{CLEAR}$ goes low; $\overline{CTS}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).

7 TRANSMIT REQUEST (TR): When set high, $\overline{RTS}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{THRE}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops).

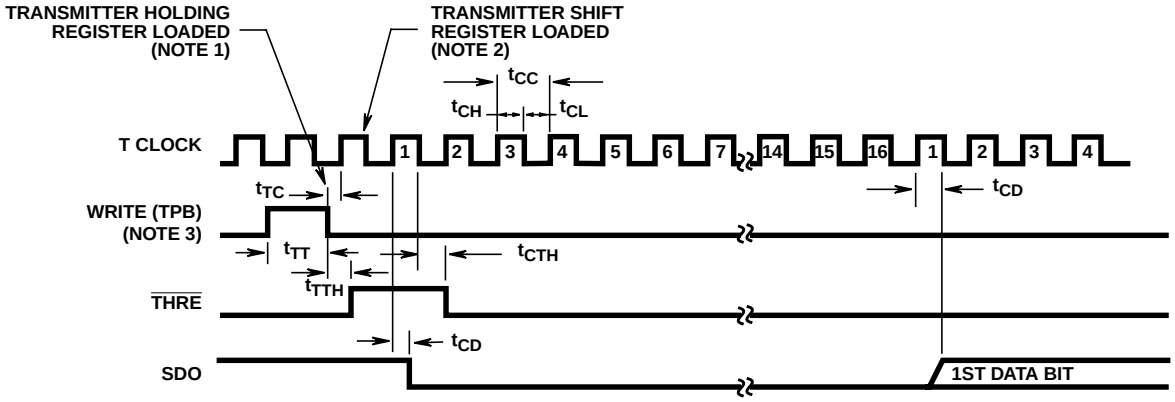
BIT 4 WLS2	BIT 3 WLS1	BIT 2 SBS	FUNCTION
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

Dynamic Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{DD} \pm 5\%$, t_R, $t_F = 20ns$, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100pF$, (See Figure 3)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A (NOTE 2) MAX	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC (NOTE 2) MAX	UNITS
TRANSMITTER TIMING - MODE 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time TPB to Clock	t_{TC}	5	175	225	175	225	ns
		10	90	150	-	-	ns
Propagation Delay Time Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	-	-	ns
TPB to $\overline{THRE}$	t_{TTH}	5	200	300	200	300	ns
		10	100	150	-	-	ns
Clock to $\overline{THRE}$	t_{CTH}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

1. Typical values for $T_A = 25^oC$ and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:

1. The holding register is loaded on the trailing edge of TPB.
2. The Transmitter Shift Register is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{TC} after the trailing edge of TPB and transmission of a start bit occurs 1/2 clock period + t_{CD} later.
3. Write is the overlap of TPB, CS1, and CS3 = 1 and $\overline{CS3}$, RD/$\overline{WR}$ = 0.

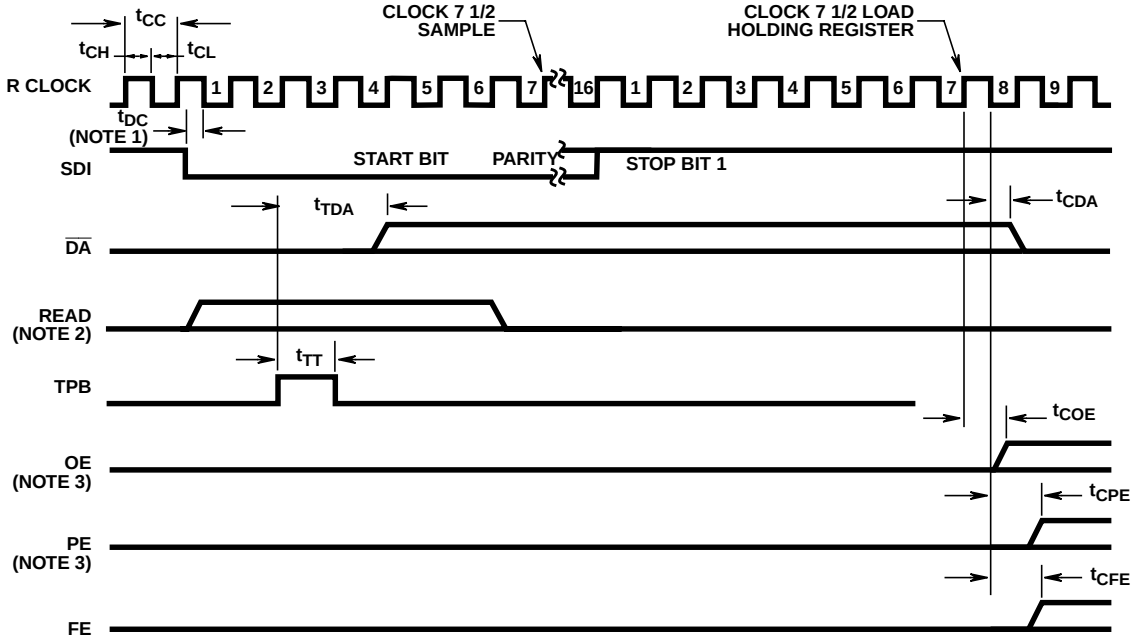
FIGURE 3. TRANSMITTER TIMING DIAGRAM - MODE 1

Dynamic Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{DD} \pm 5\%$, t_R, $t_F = 20ns$, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100pF$, (See Figure 4)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			(NOTE 1) TYP	(NOTE 2) MAX	(NOTE 1) TYP	(NOTE 2) MAX	
RECEIVER TIMING - MODE 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	220	325	220	325	ns
		10	110	175	-	-	ns
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	220	325	220	325	ns
		10	110	175	-	-	ns
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	105	150	-	-	ns
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	-	-	ns
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

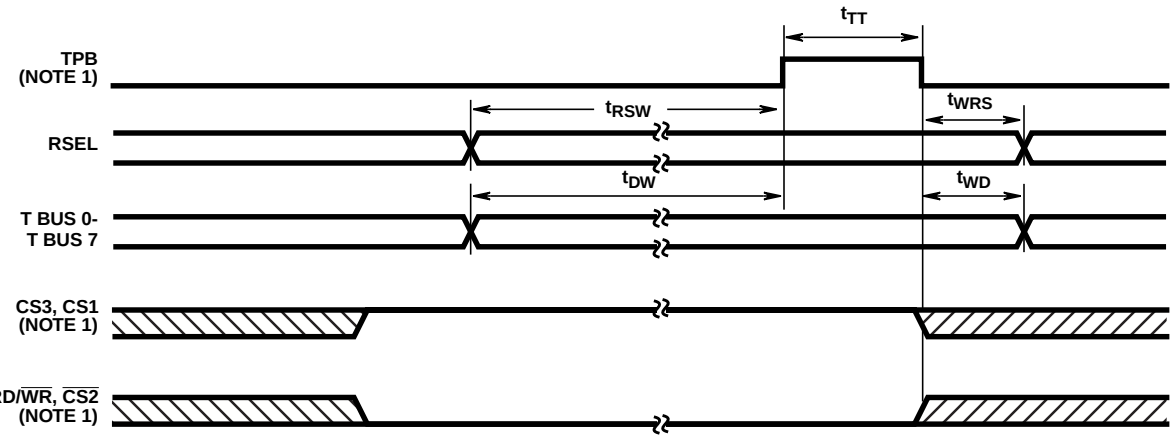
1. Typical values for $T_A = 25^oC$ and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. Read is the overlap of CS1, CS3, RD/$\overline{WR}$ = 1 and $\overline{CS2}$ = 0. If a pending DA has not been cleared by a read of the Receiver Holding Register by the time a new word is loaded into the Receiver Holding Register, the OE signal will come true.
3. OE and PE share terminal 15 and are also available as two separate bits in the status register.

FIGURE 4. MODE 1 RECEIVER TIMING DIAGRAM



NOTE:

1. Write is the overlap of TPB, CS1, CS3 = 1 and $\overline{CS2}$, RD/$\overline{WR}$ = 0.

FIGURE 5. MODE 1 CPU INTERFACE (WRITE) TIMING DIAGRAM

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 5)

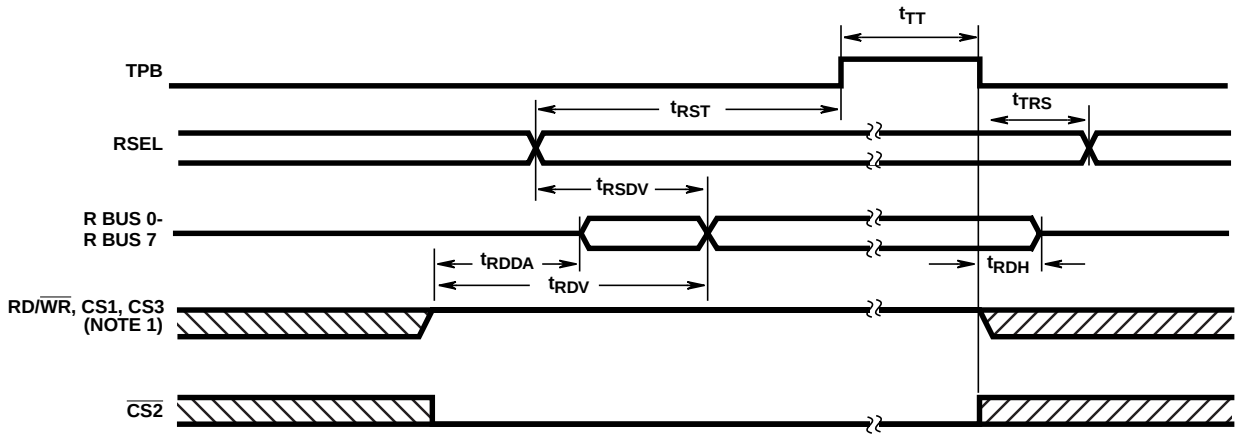
PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	CDP1854A (NOTE 2) MAX	CDP1854AC (NOTE 1) TYP	CDP1854AC (NOTE 2) MAX	UNITS
CPU INTERFACE - WRITE TIMING - MODE 1							
Minimum Pulse Width TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time RSEL to Write	t_{RSW}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Data to Write	t_{DW}	5	-30	0	-30	0	ns
		10	-15	0	-	-	ns
Minimum Hold Time RSEL after Write	t_{WRS}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Data after Write	t_{WD}	5	75	125	75	125	ns
		10	40	60	-	-	ns

NOTES:
1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 6)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A MIN	CDP1854A (NOTE 1) TYP	CDP1854A (NOTE 2) MAX	CDP1854AC MIN	CDP1854AC (NOTE 1) TYP	CDP1854AC (NOTE 2) MAX	UNITS
CPU INTERFACE - READ TIMING - MODE 1									
Minimum Pulse Width TPB	t_{TT}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
Minimum Setup Time RSEL to TPB	t_{RST}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Minimum Hold Time RSEL after TPB	t_{TRS}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Read to Data Access Time	t_{RDDA}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
Read to Data Valid Time	t_{RDV}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	
RESEL to Data Valid Time	t_{RSDV}	5	-	150	225	-	150	225	ns
		10	-	75	125	-	-	-	ns
Hold Time Data after Read	t_{RDH}	5	50	150	-	50	150	-	ns
		10	25	75	-	-	-	-	ns

NOTES:
1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTE:

1. Read is the overlap of CS1, CS3, RD/$\overline{WR}$ = 1 and $\overline{CS2}$ = 0.

FIGURE 6. MODE 1 CPU INTERFACE (READ) TIMING DIAGRAM

Mode Input Low (Mode = 0)

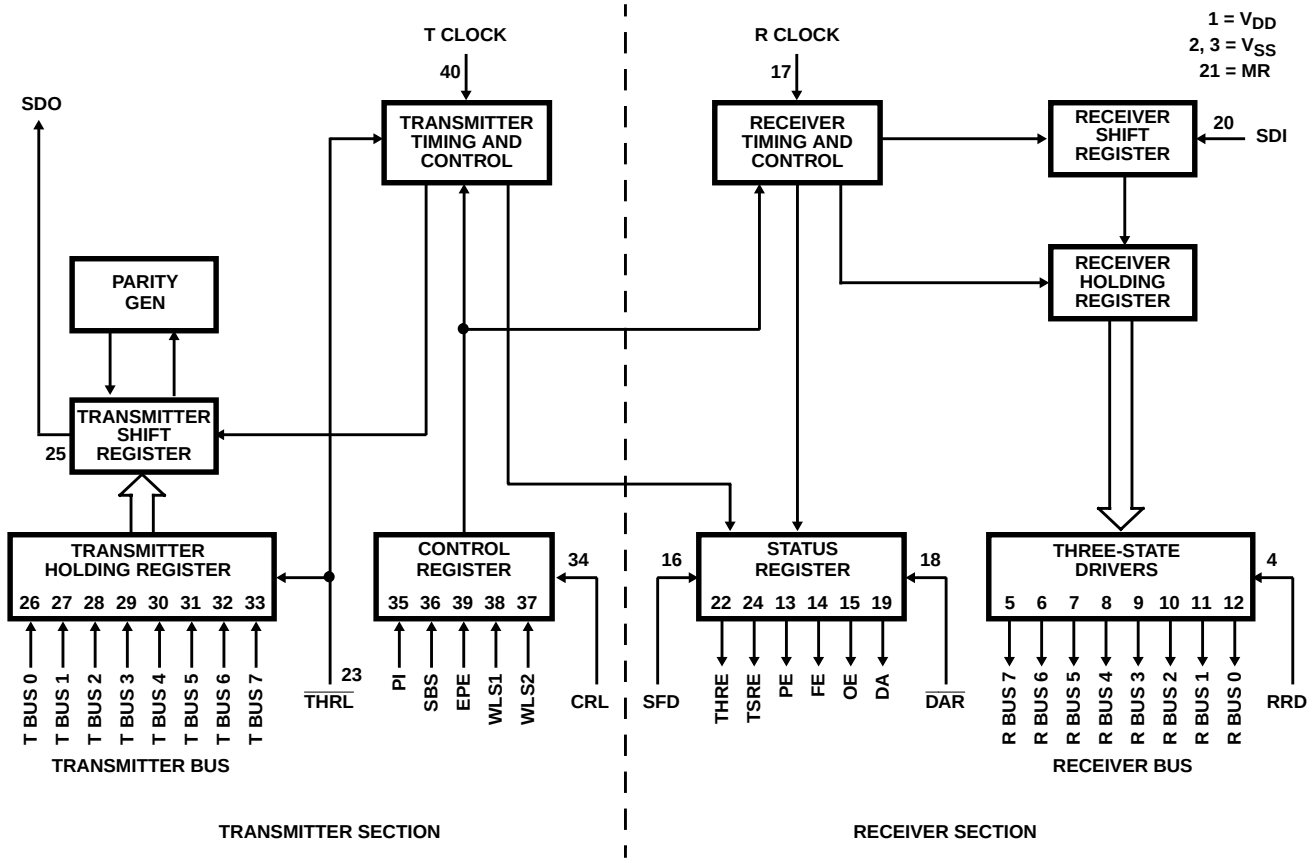


FIGURE 7. MODE 0 BLOCK DIAGRAM (INDUSTRY STANDARD COMPATIBLE)

Functional Definitions for CDP1854A Terminals Standard Mode 0

SIGNAL: FUNCTION

V_{DD}:

Positive supply voltage.

MODE SELECT (MODE):

A low-level voltage at this input selects Standard Mode 0 Operation.

V_{SS}:

Ground.

RECEIVER REGISTER DISCONNECT (RRD):

A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs.

PARITY ERROR (PE):

A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):

A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):

A high-level voltage applied to this input disables the three-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

$\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$):

A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):

A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):

A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):

A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$ ($\overline{\text{THRL}}$):

A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):

A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):

A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):

A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):

This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

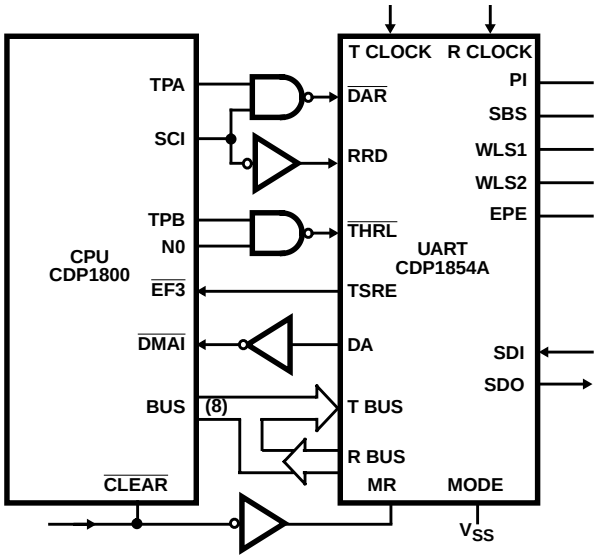


FIGURE 8. MODE 0 CONNECTION DIAGRAM

WORD LENGTH SELECT 2 (WLS2):

WORD LENGTH SELECT 1 (WLS1):

These two inputs select the character length (exclusive of parity) as follows:

WLS2	WLS1	WORD LENGTH
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):

A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

Description of Standard Mode 0 Operation (Mode Input = V_{SS})

Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A is then ready for transmitter and/or receiver operation.

Transmitter Operation

For the transmitter timing diagram refer to Figure 10. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter Holding Register by applying a low pulse to the $\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$ ($\overline{\text{THRL}}$) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins 1/2 clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high 1/2 clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Figure 12. Duration of each serial output data bit is determined by the transmitter clock frequency (^{f}CLOCK) and will be 16/f CLOCK.

Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SD line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7-1/2 in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The three-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus three-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0 - R BUS 7) outputs. Applying a negative pulse to the $\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Figure 11.

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 9)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A (NOTE 2) MAX	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC (NOTE 2) MAX	UNITS
INTERFACE TIMING - MODE 0							
Minimum Pulse Width CRL	t_{CRL}	5	100	150	100	150	ns
		10	50	75	-	-	ns
MR	t_{MR}	5	200	400	200	400	ns
		10	100	200	-	-	ns
Minimum Setup Time Control Word to CRL	t_{CWC}	5	40	80	40	80	ns
		10	20	50	-	-	ns
Minimum Hold Time Control Word after CRL	t_{CCW}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time SFD High to SOD	t_{SFDH}	5	200	300	200	300	ns
		10	100	150	-	-	ns
SFD Low to SOD	t_{SFDL}	5	75	120	75	120	ns
		10	40	60	-	-	ns
RRD High to Receiver Register High Impedance	t_{RRDH}	5	200	300	200	300	ns
		10	100	150	-	-	ns
RRD Low to Receiver Register Active	t_{RRDL}	5	100	150	100	150	ns
		10	50	75	-	-	ns

NOTES:

1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

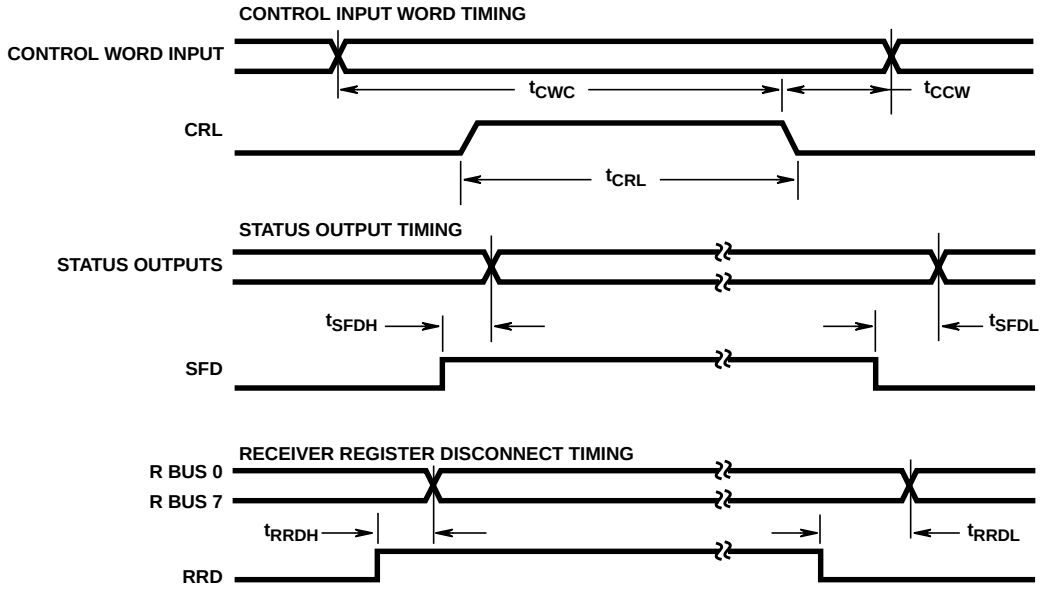


FIGURE 9. MODE 0 INTERFACE TIMING DIAGRAM

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 10)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A (NOTE 2) MAX	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC (NOTE 2) MAX	UNITS
TRANSMITTER TIMING - MODE 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{THRL}$	t_{THTH}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time $\overline{THRL}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	-	-	ns
Data to $\overline{THRL}$	t_{DT}	5	20	50	20	50	ns
		10	0	40	-	-	ns
Minimum Hold Time Data after $\overline{THRL}$	t_{TD}	5	80	120	80	120	ns
		10	40	60	-	-	ns
Propagation Delay Time Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	-	-	ns
Clock to THRE	t_{CT}	5	200	300	200	300	ns
		10	100	150	-	-	ns
$\overline{THRL}$ to THRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	-	-	ns
Clock to TSRE	t_{TTS}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

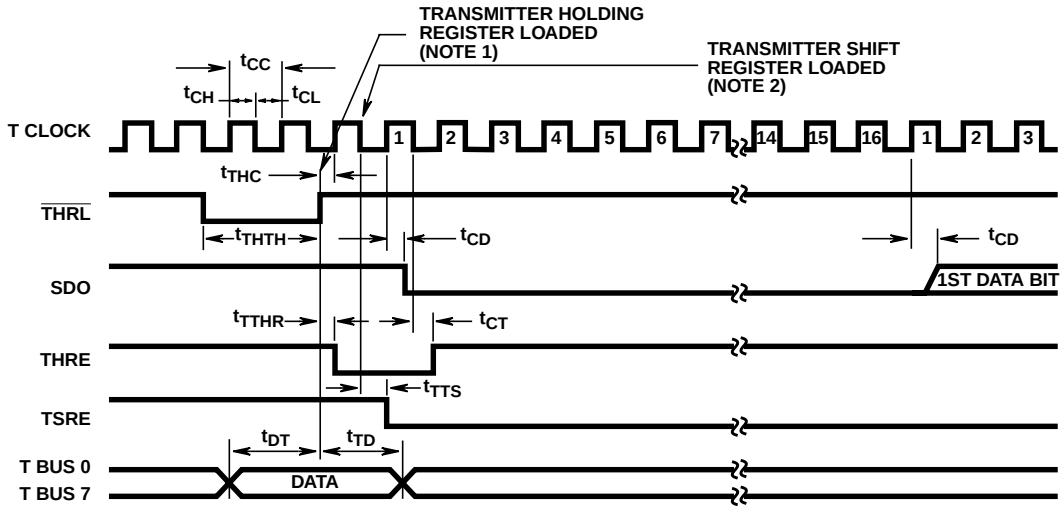
1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Dynamic Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{DD} \pm 5\%$, t_R, $t_F = 20ns$, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100pF$, (See Figure 11)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			(NOTE 1) TYP	(NOTE 2) MAX	(NOTE 1) TYP	(NOTE 2) MAX	
RECEIVER TIMING - MODE 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{\text{DATA AVAILABLE RESET}}$	t_{DD}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Minimum Setup Time							
Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time							
$\overline{\text{DATA AVAILABLE RESET}}$ to Data Available	t_{DDA}	5	150	225	150	225	ns
		10	75	125	-	-	ns
Clock to Data Valid	t_{CDV}	5	225	325	225	325	ns
		10	110	175	-	-	ns
Clock to Data Available	t_{CDA}	5	225	325	225	325	ns
		10	110	175	-	-	ns
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	100	150	-	-	ns
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	-	-	ns
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

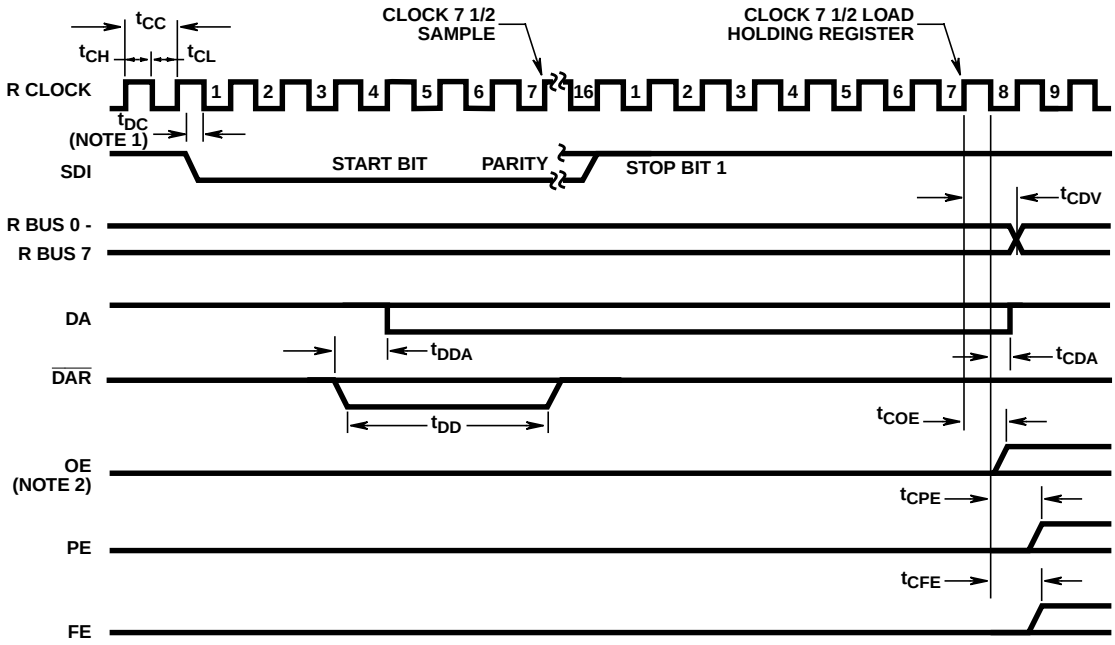
1. Typical values for $T_A = 25^oC$ and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:

1. The holding register is loaded on the trailing edge of $\overline{THRL}$.
2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{THC} after the trailing edge of $\overline{THRL}$ and transmission of a start bit occurs 1/2 clock period + t_{CD} later.

FIGURE 10. MODE 0 TRANSMITTER TIMING DIAGRAM



NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.

FIGURE 11. MODE 0 RECEIVER TIMING DIAGRAM

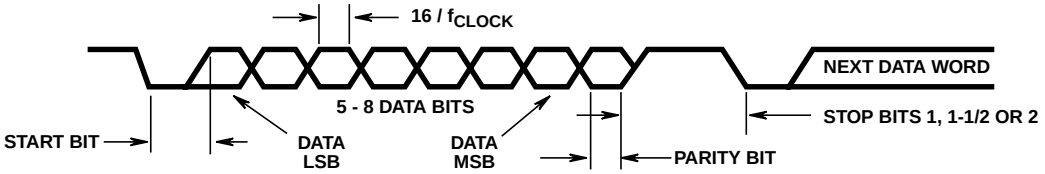


FIGURE 12. SERIAL DATA WORD FORMAT

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