

The cover of the Olivetti L1 M20 Service Manual features a grey background with a series of horizontal white stripes. A prominent orange horizontal band is positioned across the middle. The text 'M20' is printed in large, white, outlined characters within this orange band. Below the band, the words 'SERVICE MANUAL' are printed in black. At the bottom right, the brand name 'olivetti' is in a lowercase sans-serif font, followed by 'L1' in a larger, bold, uppercase sans-serif font. There are four circular punch holes along the left edge of the cover.

M20

SERVICE MANUAL

olivetti L1



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M20

SERVICE MANUAL

olivetti L1

PUBLICATION ISSUED BY:

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77, Via Jervis - 10015 IVREA (Italy)

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PREFACE

This manual is intended for field engineers.

SUMMARY

This manual describes the installation and maintenance procedures, the functional, electrical and mechanical checks, and the diagnostic procedures carried out on the M20 Basic Module.

DISTRIBUTION: Internal(Z)

REFERENCES:

Product M20	- Video General Service Manual	- Code 4100450 U
Product M20	- Spare Parts Catalogue	- Code 4100420 Z
Product M20	- Schematics	- Code 4100430 S
Product M20	- Theory of Operation	- Code 4100400 B
Product PR1450	- Service Manual	- Code 3963150 V
Product PR2400	- General Service Manual	- Code 3955010 Y(1)
Product PR1470/90	- Service Manual	- Code 3930470 Z
Product PR1480	- Service Manual	- Code 3964100 V
Product PR2300	- General Service Manual	- Code 3966450 G
Product XU4300/1	- MFDU(320KB) General Service Manual	- Code 3961640 W
Product XU4302	- MFDU(640KB) General Service Manual	- Code 3964510 W
Product XU5005	- 5.25" HDU Service Manual	- Code 3964410 V

L1M20

SERVICE MANUAL

Publication Code: 4100380 V

Date: April 1983

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FUNCTIONAL DESCRIPTION

1. FUNCTIONAL DESCRIPTION

1.1 GENERAL

The Olivetti L1 M20 professional computer is a desk top unit and in its standard configuration shown in Figure 1-1 contains two parts:

- CRT Display
- Basic Module

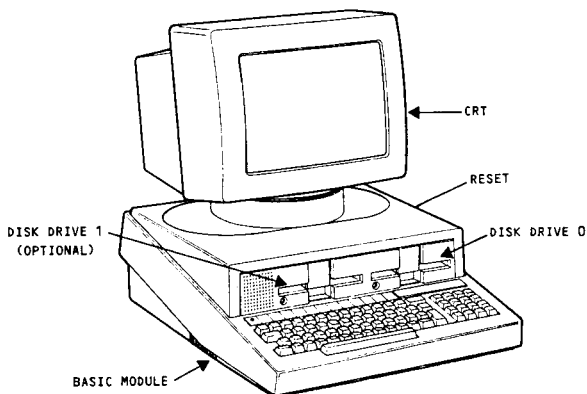


Fig. 1-1 M20 Basic Module & Display

The Display can either be a black and white (B-W) or colour 12 inch CRT. In the case of the colour Display two cables (signal and power) connect the Basic Module to the Display. An intensity control potentiometer is mounted on the back.

The Basic Module houses the motherboard, keyboard, the power supply and one 5.25 inch mini-floppy disk drive. The mini-floppy disk drive provides the ability for using magnetic media for program or data storage. Space is provided for the second optional disk drive which may be a Hard Disk Unit.

The keyboard provides an alphanumeric character set and a numeric pad. In addition, the keyboard has a power-on lamp and buzzer.

The motherboard is the printed circuit board which takes up most of the bottom of the case and contains the major circuitry for the M20 system.

It is shown in figure 1-2.

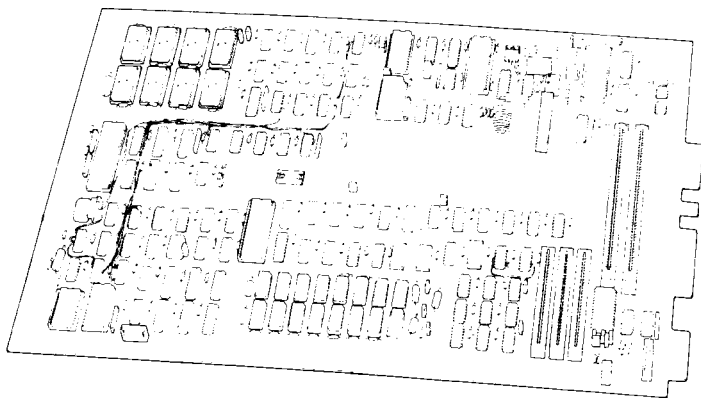


Fig. 1-2 M20 Motherboard

The motherboard holds the microprocessor (CPU), and all of the logic, memory and control circuits for peripheral interfaces (such as interface to printers), and provides space for system expansion.

A reset push button is provided to reset the M20 without the use of the power-on switch. This push button is located on the right side of the Basic module, very close to the rear, and does not extend from the cover.

Three cable connectors are provided on the back of the Basic Module for connecting to the Display and other peripheral units. The cable connectors are:

- Video connector
- Parallel Input/Output connector (Centronics-like)
- Serial Input/Output connector (RS 232C)

Space is also provided for connectors for the optional interfaces like the IEEE 488 and the TWIN RS 232C.

Figure 1-3 is a rear view of the M20 Basic Module.

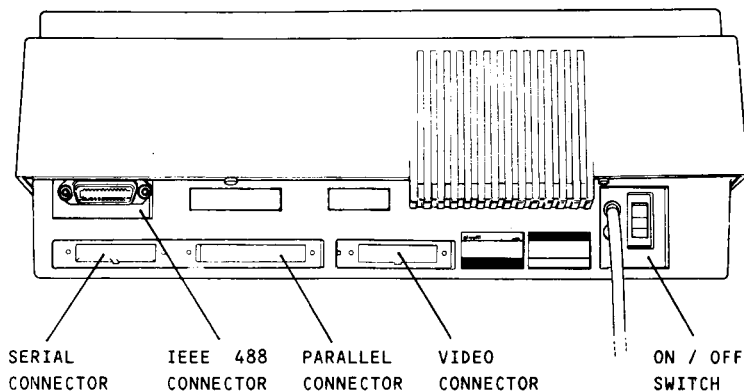


Fig. 1-3 Rear view of M20 Basic Module

1.2 SYSTEM DESCRIPTION

The following summarizes the standard configurations (CPU 1042, CPU 1049), the peripheral options supported, and the expansion options (C).

STANDARD CONFIGURATION - CPU 1042

- B-W 12" CRT Display (with graphics capability)

- Basic Module

- 72 key keyboard

- One 320 Kilobyte (KB) or 160KB or 640KB mini-floppy disk drive

- Motherboard

- Z8001 Microprocessor

- 128 KB Random Access Memory

- 8 KB Erasable Programmable Read Only Memory

- Parallel Input/Output Interface (Centronics-like)

- Dual Communication Serial Interface (RS 232C)

STANDARD CONFIGURATION - CPU 1049

- B-W 12" CRT Display (with graphics capability)

- Basic Module

- 72 key keyboard

- 1 Hard Disk unit

1 320KB or 640 KB mini-floppy disk drive
 Motherboard
 28001 Microprocessor
 128 KB Random Access Memory
 8 KB Erasable Programmable Read Only Memory
 Parallel Input/Output Interface (centronics-like)
 Dual communication serial Interface (RS 232C)

EXPANSION OPTIONS - C

Colour CRT Display
 Three 32 KB RAM Memory Expansion Boards (System Memory = 224 KB)
 or
 Three 128 KB RAM Memory Expansion Boards (System memory = 512 KB)
 Second Mini-Floppy Disk Drive (for systems with CPU 1042)
 Parallel Printers
 80 or 132 column matrix printer
 Peripheral expansion Boards
 IEEE 488 Interface Board
 TWIN RS 232C Interface Board
 Alternate Processor Board (APB) 1086(only with CPU 1042)

A simple block diagram of the M20 is shown in figure 1-4. The dotted lines show the optional features. A brief explanation of each module shown in figure 1-4 follows.

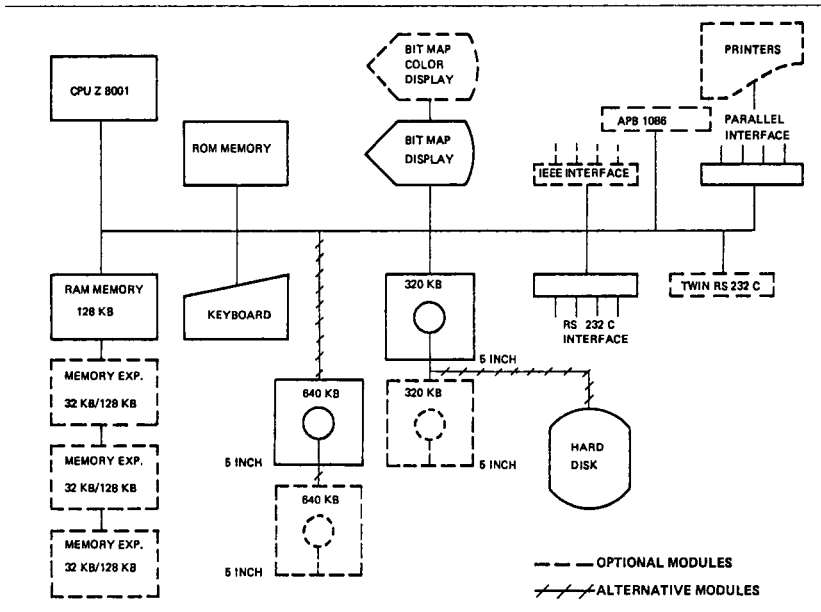


Fig. 1-4 M20 Simple Block Diagram

1.2.1 DISPLAY

In its minimum configuration the system uses a black and white Display, and a bit-mapped approach for both graphics and text. The resolution is 512 by 256 dots. The character set includes upper-case and lower-case. Standard display attributes include reverse and hide capabilities. Attributes are all software defined. Figure 1-5 shows the black and white Display.

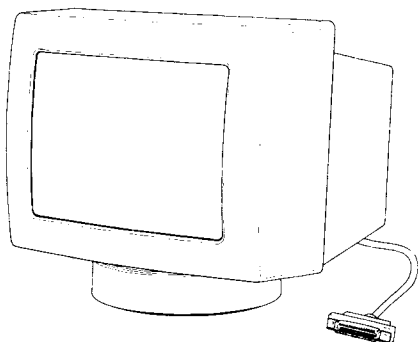


Fig. 1-5 Black & White Display

The use of the bit-map technique permits the possibility of obtaining two different video page formats (1024/2000 characters) on the same system. These formats can be selected by means of parameters. The choice of either a 1024 or 2000 character page takes place at the moment of the system start up by means of specific parameters handled by the operating system. There is no hardware difference between the two formats.

The two formats have the following characteristics:

1024 characters

characters per line: 64
number of lines: 16
net character matrix: 5 x 7
gross character matrix: 8 x 16

2000 Characters

Characters per line: 80
number of lines: 25
net character matrix: 5 x 7
gross character matrix: 6 x 10

A colour display is available as a standard option. There are two different types of colour systems:

- 4 colour
- 8 colour

In the 4 colour system eight colours are available but only four may be viewed simultaneously. In the eight colour system all the eight colours may be viewed simultaneously. The Display unit used for both systems is the same. The eight colour palette is composed of red, green, yellow, blue, magenta, cyan, black and white.

Resolution in colour is the same as in Black and White for the bit-mapped graphics but the memory requirements is higher for the colour systems. The 4 colour system requires 32 KB of RAM, the 8 colour one requires 64 KB of RAM while the Black and White only requires 16 KB of RAM.

1.2.2 VIDEO INTERFACE

The video interface provides the interface between the Display and the M20 system as well as the hardware associated with the generation of graphics and text. It is physically found on the motherboard.

1.2.3 MINI-FLOPPY DISK DRIVES

One 5.25 inch Mini-Floppy Disk Drive must always be present on an M20 system. There are three types of mini-floppy disk drives:

- 160 KB (unformatted capacity) Mini-Floppy Disk drives
- 320 KB (unformatted capacity) Mini-Floppy Disk drives
- 640 KB (unformatted capacity) Mini-Floppy Disk drives

If two mini-floppy disk drives are used, they must be of the same type. Only 320 KB or the 640 KB mini-floppy disk drives can be used as a Hard Disk back up device.

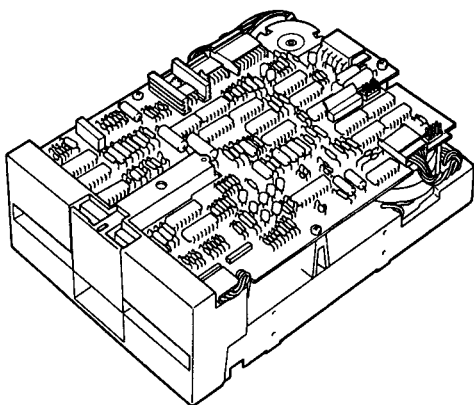


Fig. 1-6 320 KB Mini-Floppy Disk Drive

1.2.4 MINI-FLOPPY DISK INTERFACE

The mini-floppy disk interface provides two major functions for the M20 system:

- It controls the logic and control circuitry needed to control and record data onto, or to read data from the 5.25 inch mini-floppy disks
- It initially formats new disks

The mini-floppy disk interface is physically located on the motherboard.

1.2.5 MINI-FLOPPY DISK RECORD STRUCTURE

This section provides background information on the mini-floppy disk formats (320KB). A mini-floppy consists of a plastic disk, coated with magnetic media suitable for recording or storing information. Information is recorded as a series of magnetic flux reversals, on the surface of the disk. The structure is somewhat similar to a phonograph record. There are a number of separate concentric circles, called tracks holding the data. There are two moving parts: the disk which rotates continuously, and the Read/Write head which must be positioned over the selected track.

Each track is broken up into short sections called SECTORS. Each sector in double-density mode, can store 256, 512 or 1024 bytes of data. The M20 320 KB Mini-Floppy Disk drive chooses the 256 per sector drive. A byte is 8 bits long and in general can be thought of as a stream of 8 bits. On the 320 KB Mini-Floppy Disk drive there are 35 concentric tracks. Since there are 35 x 16 sectors in all, the maximum data

recording capacity is 560×256 bytes or 143.36 KB on each recording side. The total recording capacity is actually more than this, since each sector also contains data for identifying tracks and sectors, and redundancy marks for making error checks. Without the track and sector identification, data could not be recovered. Without redundancy checks, it would not be known whether errors had occurred. Track and sector information are recorded on the disk when it is formatted. In addition, one or more tracks are reserved for a directory which enables the Operating System (OS) to keep track of the files. Because the user's file may be longer than 256 bytes, a file may consist of a string of sectors, but not necessarily in sequential sectors. Directory information is "data" and is recovered in the DATA section of a sector. One or more tracks are reserved for the directory, and listing of the location of the files. Each time the OS adds or deletes a file, it also updates the directory.

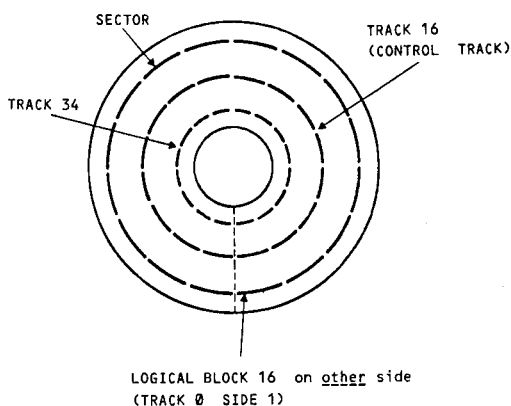


Fig. 1-7 320KB Disk Structure

1.2.6 HARD DISK UNIT

The M20 can use a 5.25 inch Winchester type Hard Disk Unit. The Hard Disk Unit is housed in the M20 Basic Module and is of the same size as the mini-floppy disk drive. The Hard Disk Unit has a storage capacity of 11.25 Mbytes (unformatted). It has three fixed platters and six read/write heads. It has 33 sectors per track, 1080 tracks and 180

cylinders. The data transfer rate is 5 Mbits per second.

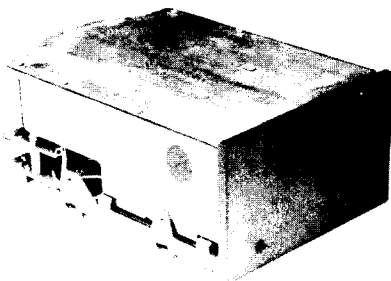


Fig. 1-8 Hard Disk Unit

1.2.7 HARD DISK CONTROLLER

The Hard Disk Controller interfaces the M20 to the Hard Disk Unit. It ensures proper operation of the Hard Disk Unit and error handling. It receives commands from the M20, decodes them, and then initializes and monitors the hardware as the command is executed and return the status back to the M20. The Hard Disk controller is physically located on two printed circuit boards:

- a board which is located under the Hard Disk Unit itself
- a small board which plugs into one of the expansion slots on the motherboard.

1.2.8 KEYBOARD-

The keyboard has 72 keys. These have been divided into two zones:

- Alphanumeric
- Numeric

There are 4 shift keys. Two grey ones (known as SHIFT) are used for the selection of upper case/lower case. There is a BLUE SHIFT (CONTROL) key which is used in combination with other characters for a variety of operations, mostly in BASIC. There is also a YELLOW SHIFT (COMMAND) which is used together with the "?/" key to provide a shift lock for the letters A-Z.

The M20 can support the following national keyboards:

- Italian (0)
- USA ASCII (4)
- French (2)

British (3)
 German (1)
 Spanish (5)
 Portuguese (6)
 Danish (8)
 Swedish and Finnish (7)
 Norwegian (11)
 Swiss - French (13)
 Swiss - German (14)
 Katakana (9)
 Greek (12)
 Yugoslavian (10)

The national keyboards are all jumper selectable (except for Greece and Yugoslavia and can be invoked by the PC05 command Set Language (SL). The numbers in parenthesis are the country codes used in the SL command. for example the command "SL 8" sets the Danish keyboard.

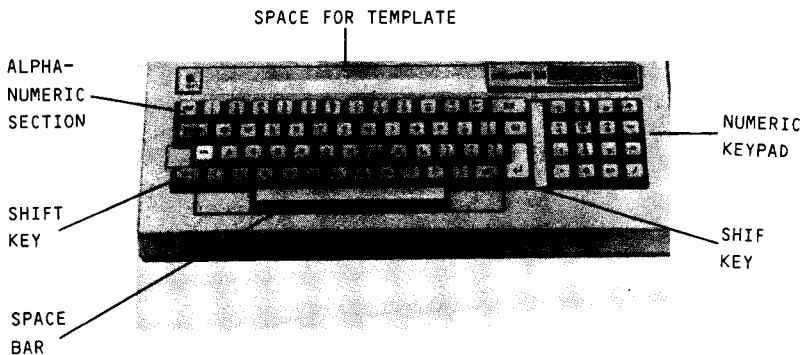


Fig. 1-9 USA ASCII Keyboard

1.2.9 DUAL COMMUNICATION SERIAL INTERFACE

The DUAL Communication Serial Interface found on the motherboard provides the M20 with one RS 232C type serial interface and one keyboard interface. The serial RS 232C interface is used to interface the M20 to a modem or plotter.

The keyboard interface provides the interface between the M20 system and keyboard.

1.2.10 CENTRAL PROCESSOR UNIT (CPU)

The M20 uses an advanced 16 bit microprocessor, the Z8001. Some of the features of the Z8001 are:

- sixteen 16 bit general registers
 - segmented addressing
 - handling of bit, byte, word and long word data
 - three types of interrupts: non-maskable, non-vector, and vectored.
- The support logic provides address translation for optimum flexibility in both hardware configuration and software utilization.

1.2.11 MEMORY (RAM and EPROM)

In the standard configuration the M20 holds 128 KB of Random Access Memory (128KB are located on the motherboard itself) and 8 KB of Erasable Programmable Read Only Memory (EPROM), also physically located on the motherboard itself.

All RAMs are dynamic and require periodic refresh. The bit-mapped black and white CRT requires 16KB of refresh RAM; the 4 colour Display requires 32 KB of refresh RAM; the 8 colour Display requires 64 KB of refresh RAM. The Basic Interpreter and Operating System (loaded from mini-floppy disk) require approximately 64 KB of RAM (loaded from mini-floppy disk). In the standard configuration usually 48 KB are available for programming use. Of this, at least 37 KB are available for user programs. The RAM memory is expandable to 224 KB by inserting three plug-in boards of 32 KB each. The RAM memory can also be expanded to 512 KB if three plug-in boards of 128 KB each are inserted instead of the 32 KB ones.

The 8 colour Display requires either two 32KB memory expansion boards or two 128KB memory expansion boards. The 4 colour display requires one 32KB memory expansion board.

The 8 KB of EPROM on motherboard contain:

- Power On Bootstrap
- Power On Diagnostics

Information in EPROM is placed there in the process of manufacturing the EPROMs. Information stored in the EPROMs as opposed to that stored in RAMs does not appear when the power is turned off.

1.2.12 PARALLEL INTERFACE

The Parallel interface provides the M20 with one Centronics-like parallel port for connecting a printer. A printer may be one of the following:

- Printer PR 2400
- Printer PR 1450
- Printer Pr 1471
- Printer PR 1481
- Printer 2300

1.2.13 TIMER

The timer is a programmable device that has three independent channels. Two of the channels are used to set the keyboard and printer baud rates. The third channel is available to the user and can be programmed as an interval real-time clock.

1.2.14 OPTIONS

The options on the M20 are:

- IEEE 488 Interface Board
- TWIN RS 232C Interface Board
- Alternate Processor Board (APB) 1086

All of the above options may be plugged into slots J3 or J4 on the motherboard.

1.2.14.1 IEEE 488

The IEEE (Institute of electrical and Electronic Engineers) 488 board provides a means to transfer digital data among a group of instruments and system components. As implemented in the M20, the IEEE option consists of a plug-in miniboard containing six integrated circuits providing TALKER, LISTENER and CONTROLLER functions plus line transceivers. It can be used with systems that use a byte-serial means of data transfer. These interface functions are described below.

LISTENER - A device capable of receiving data over the interface when addressed. Examples of this type of device are printers, display devices, programmable power supplies, programmable signal sources and the like.

TALKER - A device capable of transmitting data over the interface when addressed. Examples of this type of device are tape readers, voltmeters that are outputting data, counters that are outputting data and so on.

CONTROLLER - A device capable of specifying talkers and listeners for data transfer. Examples of this are computers like the M20.

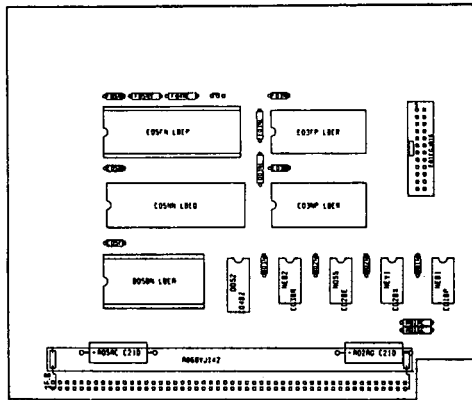


Fig. 1-10 IEEE 488 Board

1.2.14.2 Twin RS 232C Interface Board

This interface board provides two communication channels with both RS 232C and 20mA current loop option. It supports asynchronous and synchronous communication and various BAUD rates are easily programmable for each channel. The use of an intelligent interrupt controller enables a real type of software capabilities. The board is provided with capabilities of both receiving and transmitting the transmit and receive data clocks for the synchronous communications. The board can be configured as follows:

- 2 RS 232C Channels
- 2 Current Loop Channels
- 1 RS 232C Channel and 1 Current Loop Channel

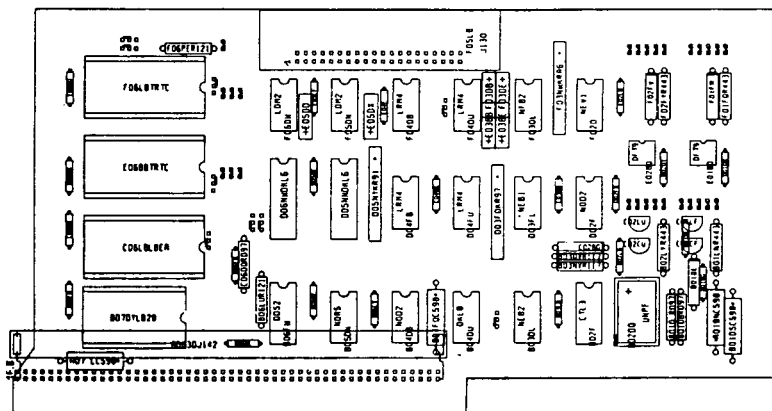


Fig. 1-11 Twin RS 232C Board

1.2.14.3 Alternate Processor Board 1086

The Alternate Processor Board (APB) 1086 is a plug in board which allows the M20 to execute software written for an Intel 8086 microprocessor. The purpose of this board is to support the following two widely used operating systems:

CP/M 86

MS-DOS

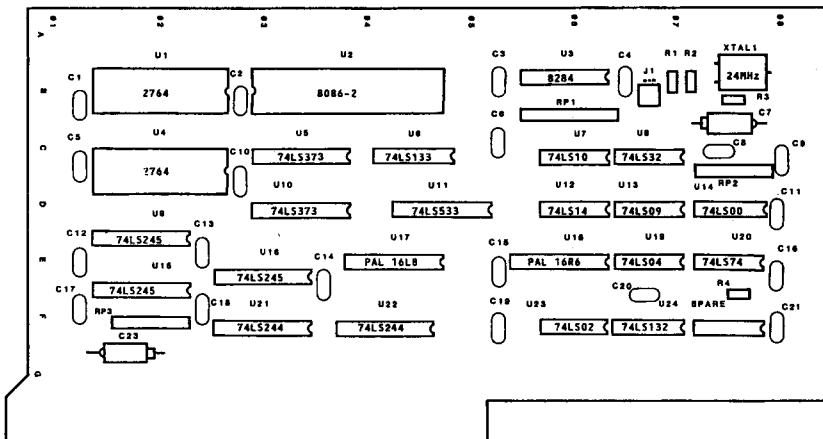


Fig. 1-12 APB 1086 Board

1.2.15 POWER SUPPLY

The M20 power supply is housed in a metal case inside the Basic Module. It provides the correct power source to all L1 M20 circuitry. It is a switching type of power supply. A voltage selector jumper is present in the power supply. This jumper selects one of the following AC line input voltages:

100 - 120 Volts A.C.

200 - 240 Volts A.C.

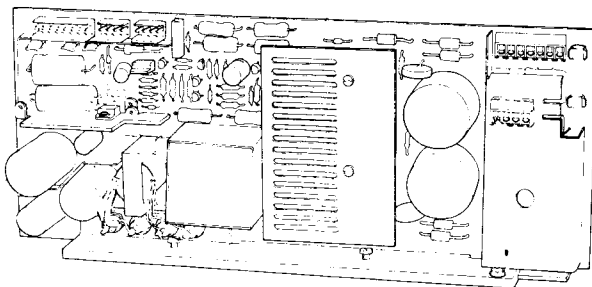


Fig. 1-13 M20 Power Supply

1.2.16 EXTERNAL HARD DISK UNIT

The external hard disk unit is an optional feature which can be added to an M20 with a configuration of 2 minifloppy disk drives. It resides in a separate case placed beside the M20. The H.D.U. module include:

- the XU 5005 5.25" Hard Disk Unit
 - a power supply unit which provides power to the HDU
 - a small interface board IF162
-

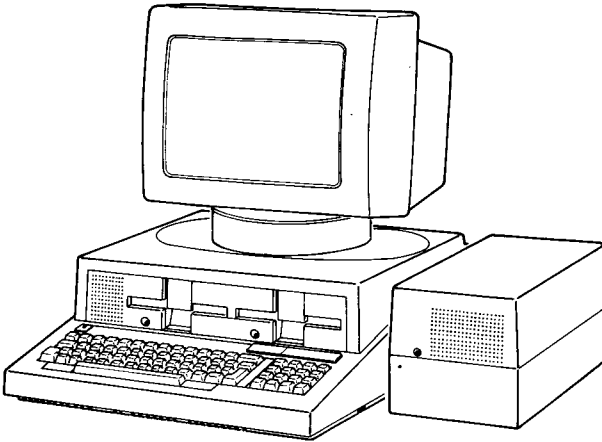


Fig. 1-13 The M20 with the External Hard Disk Unit Module

The aim of the external H.D.U is to increase the disk capacity of the M20 by another 11.25 Mbytes (unformatted).

The external H.D.U. is connected to the M20 via the Hard Disk Controller G0223 which resides at the bottom of the floppy disks assembly and via the transition board which plugs into the connectors J3 or J4 of the motherboard. These two boards are the same boards used to interface the internal hard disk unit to the M20 although two modifications have to be made on each board.

The H.D.U. module has its own power supply unit and does not use the M20's power supply.

Also an LED on the front of the H.D.U. module is present to indicate that the disk unit is selected.

The function of the interface board IF162 is to inhibit any data to be written on the disk drive while the M20 is being switched on or off.

The software and diagnostic procedures relative to the integrated hard disk unit are still valid for the external hard disk unit.

1.2.17 TV ADAPTER

The TV adapter is a device which permits the connection of one or more TV sets to the M20. It can be used with the PAL system (in Europe) as well, as with the NTSC system (in USA).

Its principal characteristics are as follows:

NTSC VERSION

1. Video resolution 256 dots x 200 lines
 42 characters x 19 lines
2. TV signal NTSC format
3. TV set 525 cycle/60 Hertz

PAL VERSION

1. Video resolution 256 dots x 232 lines
 42 characters x 25 lines
2. TV signal PAL format
3. TV set 625 cycle/50 Hertz

The minimum number of colours that can be visualised at a time is 4 while the maximum number is 16. The choice is done from a palette of 512 colours.

INSTALLATION AND UPGRADES

2. INSTALLATION AND UPGRADES

2.1 INTRODUCTION

This chapter deals with the site preparation, environmental requirements, installation procedures, printer jumper charts, upgrades, jumper charts for the various boards and motherboard, and connector descriptions.

2.2 SITE PREPARATION

The M20 operates reliably in a typical office environment but it is important to adhere to the following points when choosing a suitable site:

1) THE M20 SHOULD BE PLUGGED INTO AN EARTHED POWER SUPPLY. Unearthed machines do not work properly and can be a safety hazard. If the M20 is not plugged into an earthed circuit one can experience:

- improper program operation
- unreadable disks
- expensive machine damage

The M20 should when possible be isolated from sources of electrical noise, and from devices that can cause excessive voltage level variations. Some common sources of electrical noise are:

- air conditioners, fans and large blowers
- transformers and alternators
- large brush type or induction motors such as those used on elevators
- radio and TV transmitters, signal generators and high frequency security devices

Note: Some of the normal small office machines (typewriters, small copiers, calculators etc) are allowed on the same line provided that they do not cause excessive interference on the line.

2) The M20 should be placed in a relatively dust-free place. Airborne dust, dirt and smoke can cause excess wear on moving surfaces, short and open circuits (especially in the presence of high humidity) and read/write errors on the disk.

3) The M20 should be placed away from heat and direct sunlight. Unusually high temperatures coupled with low humidity can cause static problems.

4) The M20 is cooled by a fan at the rear. This area must be kept clear of papers or other materials that would obstruct air flow.

2.3 INPUT AC ELECTRICAL CHARACTERISTICS

The M20 input electrical characteristics are listed below.

- 1) Monophase, alternating voltage with the following nominal voltages: 100 to 120 Volts or 200 to 240 Volts. The voltage ranges are jumper selectable in the power supply itself.
- 2) Permanent driftings of input voltage: +10%, -10% Consequently the two ranges of operation are: 90 Volts to 132 Volts; 180 to 264 Volts.
- 3) Nominal frequency : 50Hz or 60Hz with the same model without any variation.
- 5) Frequency driftings +5%, -5%

2.4 OUTPUT DC ELECTRICAL CHARACTERISTICS

VOLTAGE	TOLERANCE	CONTINUOUS CURRENT MIN/MAX	MAX RESIDUAL RIPPLE
+ 5 Volts	5%	3.3/8.9 Amperes	50mVp-p
+ 12 Volts	3%	2.0/6.2 Amperes	100mVp-p
- 12 Volts	5%	.03/.7 Amperes	100mVp-p

2.5 ENVIRONMENTAL REQUIREMENTS

Operating Environment:

temperature: 10 degrees to 40 degrees Centigrade (50 to 104 F)

relative humidity: 10% to 95%

Nonoperating Environment

temperature: 5 degrees to 45 degrees Centigrade (41 to 113 F)

relative humidity: 5% to 95%

Heat Dissipation: 140 watts (477.7 BTU/hour)

2.6 PHYSICAL CHARACTERISTICS

WEIGHT

Basic Module:

with one mini-floppy disk drive 9.2Kg (20.24lbs)

with two mini-floppy disk drives 11Kg (24.2lbs)

with one mini-floppy disk drive and Hard Disk 11.6Kg (25.6lbs)

Display: 9 Kg (19.8lbs)

PHYSICAL DIMENSIONS

Basic Module:

Width: 43cm (17.2in); height: 15.5cm (6.2in); depth: 51.9cm (20in)

Display:

Width: 33.4cm (13.36in); height: 26cm (10.4in); depth 31cm (12.4in)

2.7 INSTALLATION

This section describes how the M20 computer system should be installed. To ensure a smooth, easy set-up one has to adhere to the following instructions carefully.

2.7.1 CONNECTING THE BLACK & WHITE DISPLAY TO THE BASIC MODULE

The Black and white Display is connected to the Basic Module by means of a single cable. One end of this cable is already fastened to the display. The other end has a connector with two screws at the edges. This connector fits into the edge connector at the rear of the Basic Module as shown in figure 2-1. This edge connector on the motherboard is J5.

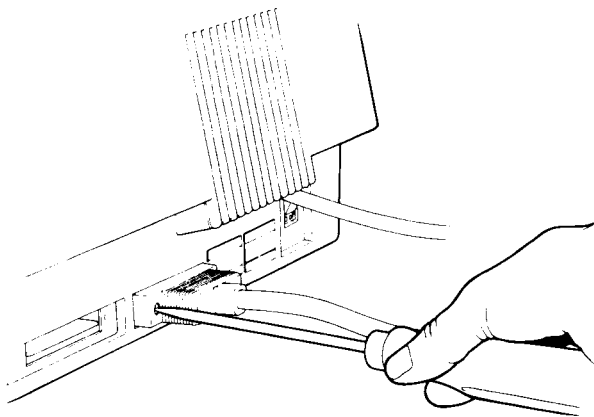


Fig. 2-1 Installing the B/W Display

The connector at the end of the cable is referred to as P5. The

connector P5 cannot be fitted the wrong way as a plastic key inside the connector prevents this. The two screws at the edge of P5 are then tightened so as to firmly seat P5 into position.

2.7.2 CONNECTING COLOUR DISPLAY TO THE BASIC MODULE

The colour Display is connected to the Basic Module by means of two cables:

- Power Cable (A)
- Signal Cable (B)

See figure 2-2 below.

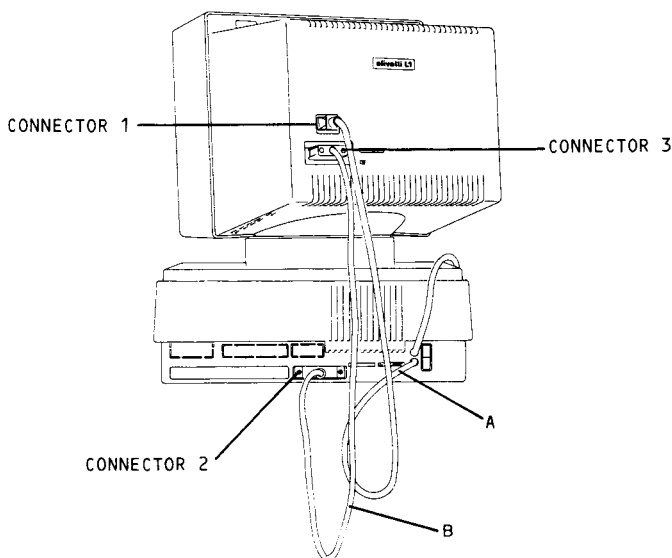


Fig. 2-2 Installing the Colour Display

One end of the power cable A is already fastened to the Basic Module and exits from the bottom hole to the left of the ON/OFF switch at the rear of the Basic Module. The other end of this cable plugs into the top connector (connector 1) at the back of the Colour Display. One end of the signal cable (connector 2) has a connector with two screws at the edges. This connector 2 fits into the edge connector at the rear of the Basic Module. This connector cannot be fitted the wrong way round as a plastic key inside the connector 2 prevents this. The two screws at the edge of connector 2 are then tightened with a screwdriver so as to firmly seat the connector in position.

The other end of this signal cable has a connector (connector 3) which fits at the back of the Display. This slot has two locking springs to clamp connector 3 firmly in position.

NOTE: For 4 colour systems 1 colour memory expansion board must be plugged into the M20 motherboard. For 8 colour systems, 2 colour memory expansion boards must be plugged into the M20 motherboard. See the table below.

CONFIGURATION	Z1-Z22	K1-K2	E1-E2	V1-V2	W1-W2	M1-M2	X1 - X8	X2 - X7	X3 - X6	U62/3/4/5	U86 A
M 20 WITH OUT ANY EXPANSION BOARDS	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	ON	OFF	ICs PRESENT	OFF
M 20 WITH AT LEAST ONE B/W 32KB EXPANSION BOARD	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	OFF	OFF	ICs PRESENT	OFF
M 20 WITH AT LEAST ONE B/W 128KB EXPANSION BOARD	Z - Z1	K - K1	E - E1	V - V2	W - W1	M - M2	ON	OFF	OFF	ICs NOT PRESENT	ON
M 20 WITH ONE 32KB COLOUR BOARD (4 COLOURS)	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	OFF	ON	ICs PRESENT	OFF
M 20 WITH ONE 128KB COLOUR BOARD (4 COLOURS)	Z - Z1	K - K1	E - E1	V - V2	W - W1	M - M2	OFF	ON	ON	ICs NOT PRESENT	ON
M 20 WITH TWO 32KB COLOUR BOARDS (8 COLOURS)	Z - Z1	K - K2	E - E2	V - V1	W - W2	M - M1	ON	OFF	ON	ICs PRESENT	OFF
M 20 WITH TWO 128KB COLOUR BOARDS (8 COLOURS)	Z - Z1	K - K1	E - E2	V - V2	W - W1	M - M2	ON	ON	ON	ICs NOT PRESENT	ON

2.7.3 CONNECTING A PRINTER TO THE SYSTEM

Parallel printers are connected to the M20 via the Centronics-like parallel interface. The jumper charts for the five types of printers are given in sections 2.6.3.1 to 2.6.3.7. The cable used for such a connection is the same for all printers. The connector on one end of the cable plugs into the edge connector of M20 J6. This connector on the end of the cable has two screws at the edges. The other connector at the other end of the cable fits into the connector at the back of the printer. The connection to the M20 is shown in figure 2-3. The mains cable of the printer has to be connected to a suitable power outlet. AFTER ONE HAS VERIFIED THAT THE VOLTAGE INDICATED ON THE STICKER OF THE PRINTER INDICATES THE SAME VOLTAGE AS THE POWER OUTLET GOING TO BE USED.

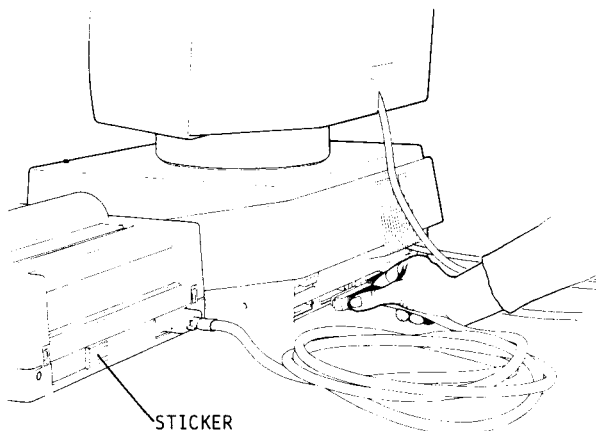
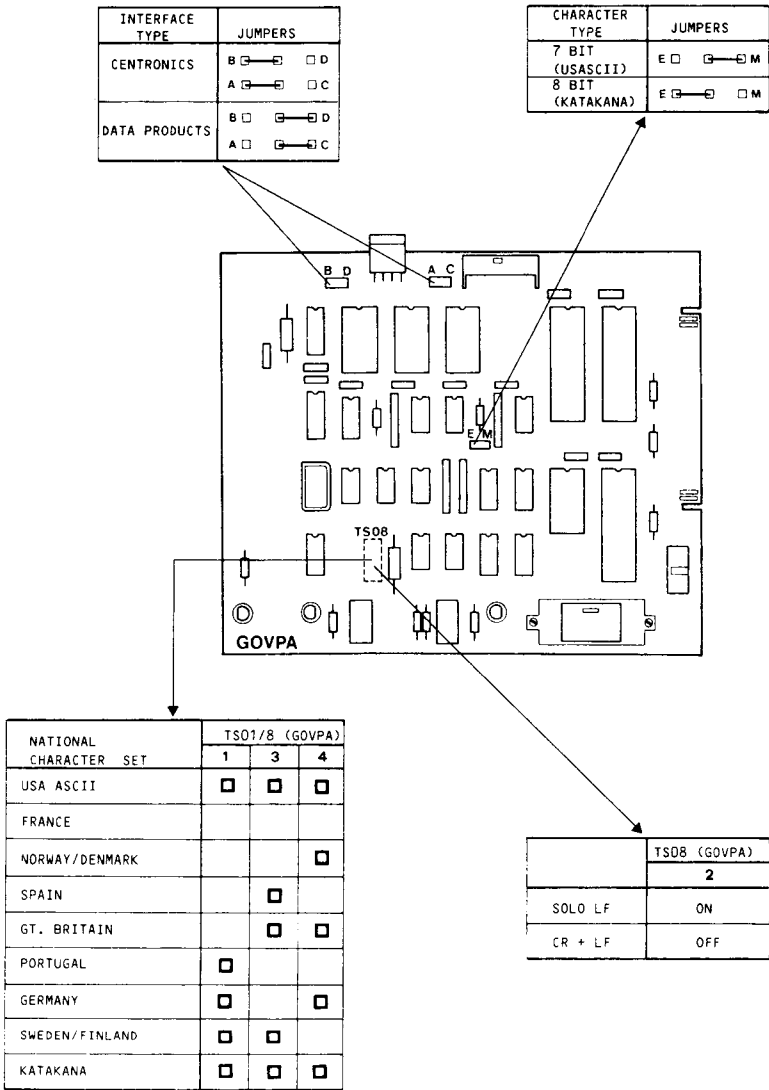


Fig. 2-3 Connecting Printer to Basic Module

2.7.3.1 PR 2400 GOVPA Jumper Settings



☒ = DIPSWITCH ON

2.7.3.2 PR 1450 Jumper Settings

Board BA056

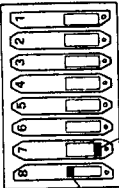
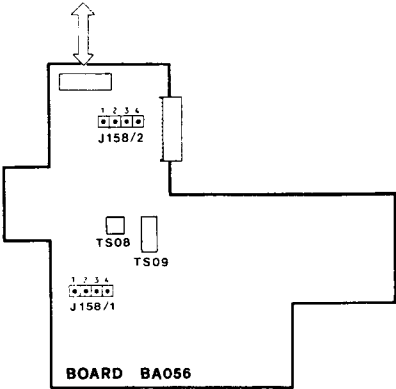
OPTIONAL VARIANTS	TS09					
	1	2	3	4	5	6
NOT USED	-					
AUTO LF ON		☒				
AUTO LF OFF		☐				
MODULO 4"			☒	☒		
MODULO 8.5"				☒		
MODULO 11"			☒			
MODULO 12"						
16.6 CHAR/INCH					☒	
10 CHAR/INCH						
PRINT III						☒
IGNORES UNKNOWN CHARACTER						

☒ = DIPSWITCH ON

NATIONAL CHARACTER SET	TS08			
	1	2	3	4
SPAIN			☒	☒
INTERNATIONAL	☒	☒	☒	☒
GERMANY		☒	☒	☒
PORTUGAL	☒		☒	☒
DENMARK/NORWAY	☒	☒		☒
FRANCE		☒		☒
ITALY	☒			☒
SWEDEN/FINLAND				☒
GT. BRITAIN		☒	☒	
USA ASCII	☒		☒	
SWITZERLAND	☒	☒	☒	

☒ = DIPSWITCH ON

DIPSWITCHES TSxx E PONxx

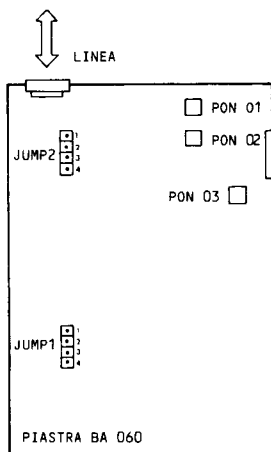


POSIZIONE "0" INTERUTTORE OFF
POSIZIONE "0" SWITCH OFF

POSIZIONE "1" INTERUTTORE ON
POSIZIONE "1" SWITCH ON

SWITCH	JUMPERS	FUNCTION
J158/1	1 - 2	DIAGNOSTIC FOR PARALLEL VERSION
	3 - 4	DIAGNOSTIC FOR SERIAL VERSION
J158/2	1 - 2	8 BIT FORCED TO ZERO
	3 - 4	8 BIT OF THE LINE

Board BA060



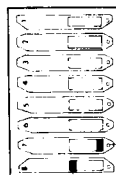
VARIANTI PRESTAZIONALI Optional Variants	PON 01 1 2 3 4			
MODULO 4" Module 4"	1		1	
MODULO 8.5" Module 8.5"	0		1	
MODULO 11" Module 11"	1		0	
MODULO 12" Module 12"	0		0	
16.6 CAR/INCH				1
10 CAR/INCH				0
STAMPA III - Print III		1		
IGNORA CAR.SCONOSCIUTO Ignores unknown char.		0		

PONTICELLO Jumper	PONTICELLATO IN Jumper Connection	FUNZIONE Function
JUMP 1	1 - 2	DIAGNOSTICA PER VERSIONE PARALLELA Diagnostic for Parallel Version
	3 - 4	DIAGNOSTICA PER VERSIONE SERIALE Diagnostic for Serial Version
JUMP 2	1 - 2	8° BIT DA LINEA 8th bit from Line
	3 - 4	8° BIT FORZATO A ZERO 8th bit forced to zero

SET GRAFICO-VARIANTI NAZIONALI Graphic Set-National Variants	PON 02 1 2 3 4			
INTERNAZIONALE International	1	1	1	1
GERMANIA Germany	1	1	1	0
PORTOGALLO Portugal	1	1	0	1
SPAGNA Spain	1	1	0	0
DANIMARCA - NORVEGIA Denmark - Norway	1	0	1	1
FRANCIA France	1	0	1	0
ITALIA Italy	1	0	0	1
SVEZIA - FINLANDIA Sweden - Finland	1	0	0	0
REGNO UNITO United Kingdom	0	1	1	0
USA - ASCII Usa - ASCII	0	1	0	1
SVIZZERA Switzerland	0	1	1	1

VARIANTI PRESTAZIONALI Optional Variants	PON 03 1 2	
IGNORA CR ON		1
IGNORE CR OFF		0
AUTO LF ON	1	
AUTO. LF OFF	0	

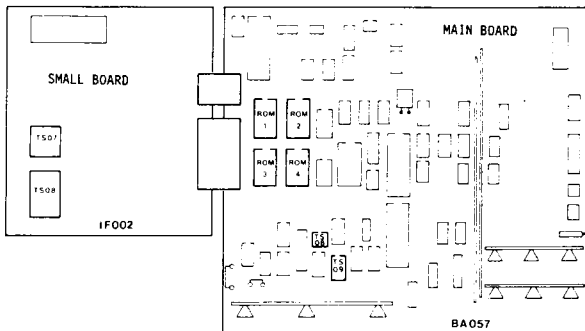
DIPSWITCHES TSxx E PONxx



POSIZIONE "0"
INTERRUPT. OFF
"0" position
switch OFF

POSIZIONE "1"
INTERRUPT. ON
"1" position
switch ON

2.7.3.3 PR 1471 Jumper Settings



		IF002 TS08			
		4	1	2	3
INTERFACE CENTRONICS	☐				
INTERFACE DATA					
RAM 0 K			☐	☐	
RAM 2 K		☐			
RAM 4 K		☐		☐	

		IF002 TS07	
		1	2
7 BITS	☐		
8 BITS		☐	

☐ = DIPSWITCH ON

OPTIONAL VARIANTS	BA052 - BA057 TS09			
	1	2	3	4
CR AFTER LF	☐			
SECOND SIGNAL FOR UNKNOWN CHARACTER		☐		
LF AFTER CR			☐	
LOCAL SETTING FOR BEL				☐

☐ = DIPSWITCH ON

FORMS TYPE	BA052 - BA057 TS08			
	1	2	3	4
DISABLE VERTICAL PROGRAMMING				
SPECIAL FORMS	☐			
SPECIAL FORMS		☐		
FORMS 3"	☐	☐		
FORMS 4"			☐	
FORMS 5"	☐		☐	
FORMS 6"		☐	☐	
FORMS 7"	☐	☐		
FORMS 8"				☐
FORMS 9"	☐			☐
FORMS 10"		☐		☐
FORMS 11"	☐			☐
FORMS 12"			☐	☐
FORMS 13"	☐		☐	☐
FORMS 14"		☐	☐	☐
FORMS 8.5"	☐	☐	☐	☐

☐ = DIPSWITCH ON

NATIONAL CHARACTER SET	TS09			
	5	6	7	8
SPAIN			☐	
USA ASCII				
INTERNATIONAL	☐			
GERMANY		☐		
PORTUGAL	☐	☐		
DENMARK/NORWAY	☐		☐	
FRANCE		☐	☐	
ITALY	☐	☐		
SWEDEN/FINLAND				☐
SWITZERLAND	☐			☐
GT. BRITAIN		☐		☐
USA ASCII/2	☐	☐		☐
YUGOSLAVIA			☐	☐
ICELAND	☐		☐	☐
JAPAN		☐	☐	☐
RESERVED	☐	☐	☐	☐

☐ = DIPSWITCH ON

2.7.3.4 PR 1481 Jumper Setti

SCELTA).

SU PIASTRA INTERFACCIA IF002
the Interface Board IF002SET GRAFICO - VARIAN
Graphic Set - Country

NAZIONE Country		
(CRT 300) ROM A	(CRT 301) ROM B	NAZIONE SW 1
U.S.A. ASCII	GRECIA Greece	
INTERNAZIONALE International	RUSSIA 1	ON
GERMANIA Germany	RUSSIA 2	
PORTOGALLO Portugal	RISERVATO Reserved	ON
SPAGNA Spain	SET GRAFICO Graphic set	
DANIM./NORV. Denmark/Norway	RISERVATO Reserved	ON
FRANCIA France	RISERVATO Reserved	
ITALIA Italy	RISERVATO Reserved	ON
SVEZIA/FINLAN. Sweden/Finland	GRECIA Greece	
SVIZZERA Switzerland	RUSSIA 1	ON
GRAN BRETAGNA G. Britain	RUSSIA 2	
U.S.A. ASCII	RISERVATO Reserved	ON
JUGOSLAVIA Yugoslavia	SET GRAFICO Graphic set	
ISLANDA Iceland	RISERVATO Reserved	ON
GIAPPONE Japan	RISERVATO Reserved	
RISERVATO Reserved	RISERVATO Reserved	ON

ESTENSIONE RAM DI LINEA
Memory Capacity

SEGNALI SU TS08 Signals on TS08		
1MM03 SW1	1MM02 SW2	1MM01 SW3
ON		

FORMATO CARATTERE
Character Format

BIT DI CODICE Code bit	SEGNALI SU TS07 Signal on TS07	
	DATAX SW1	DATAX SW2
7. BIT	ON	OFF
8. BIT	OFF	ON

VARIANTI PRESTAZIONE
Operational Variants

VARIANTE Variant	CR/LFO SW 1	SC SI
FORZA CR DOPO MOVIMENTO CARTA Carriage return after line feed	ON	
COMPATTA MESSAGGIO PER CARATTERE SCONOSCIUTO Message packing in event of unknown character		
FORZA-LF DOPO CR Line feed after carriage return		
PONI LOCALE PER BELL Local for bell code		

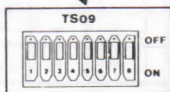
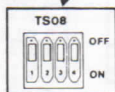
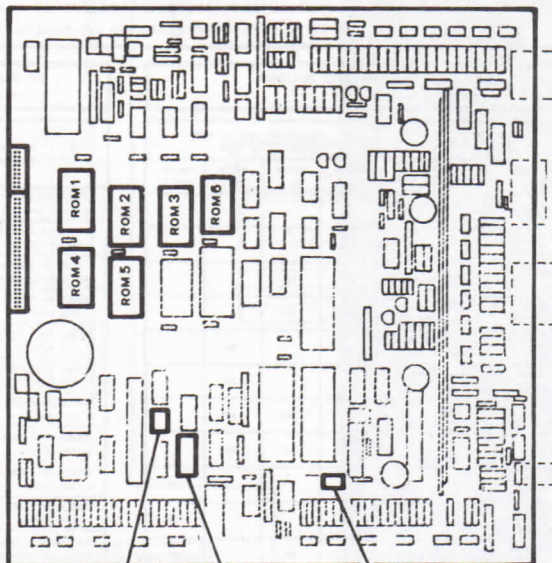
TIPO INTERFACCIA
Interface Type

TS08-SW4	
CENTRONICS	ON
DATA PRODUCTS	OFF

Mov.	Data	Mov.	Data	Viato <i>2/2</i>	Viato <i>1/2</i>
				Sequenza sul loglio N° 2/2	N° loglio 1/2
Codice				a	Buff
6	2	7	4	6	1
				U	

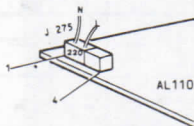
PRINTED IN ITALY BY OLIVETTI MKTG/DT - IVREA

PIASTRA GOVERNO BA065
Control Board BA065



PREDISPOSIZIONI SU AL110
Presetting on AL110

TENSIONE RETE Mains Voltage	J125 AL110
200 - 240 VAC	1 - 2
100 - 120 VAC	3 - 4



N° foglio	Codice	«	Suff.
2/2	6 2 7 4 6 1	U	

2.7.3.5 PR 2300 Jumper Settings

IL PRESENTE CARTELLINO DEVE ESSERE COMPILATO ALL'ATTO DELL'INSTALLAZIONE (APPORRE UNA "X" IN CORRISPONDENZA DELLA CONFIGURAZIONE SCELTA).
THIS CARD SHOULD BE COMPILED DURING INSTALLATION (ENTER "X" NEXT TO CONFIGURATION CHOSEN).

RELEASE MICROPROGRAMMA
FIRMWARE RELEASE

GENERATORE CARATTERI
CHARACTERS GENERATOR

DI LINEA
CIA
OR FOR
FACE

CONNETTORE DI LINEA
PER INTERFACCIA
PARALLELA
LINE CONNECTOR FOR
PARALLEL INTERFACE

STB	1	10
DATA 1		20
DATA 2		
DATA 3		
DATA 4	5	
DATA 5		
DATA 6		25
DATA 7		
DATA 8		
ACK		
BUSY	10	
PE		30
SELECT		
GND		NC
NC	15	GND
GND		NC
+5	10	30
		NC

PREDISPOSIZIONE
PRESETTING OF

MODALITA' SCAMBIO DATI
DATA EXCHANGE PROCEDURE

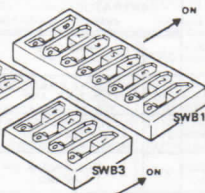
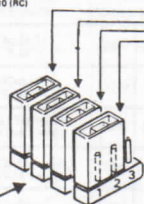
CON O SENZA PROTOCOLLO WITH OR WITHOUT PROTOCOL	DIP SWITCH SWB2
SENZA PROTOCOLLO PROTOCOL NOT SELECTED	ON
CON PROTOCOLLO PROTOCOL SELECTED	OFF
PROTOCOLLO ETX - ACK ETX - ACK PROTOCOL	OFF ON
PROTOCOLLO XON - XOFF XON - XOFF PROTOCOL	OFF OFF

PREDISPOSIZIONI SPECIFICHE PER RS 232 C
SPECIFIC PROGRAMMING FOR RS 232 C

GESTIONE SEGNALI DI INTERFACCIA SIGNALS INTERFACE HANDLING	PONTI JUMPER
UC FORNISCE CTS (CLEAR TO SEND) CU GIVES CTS (CLEAR TO SEND)	PON 1
UC NON FORNISCE CTS CU DOES NOT GIVE CTS	PON 2
SEGNALAZIONE OCCUPATO SU TD (TRANSMITTED DATA) OCCUPIED ON TD	1 -
SEGNALAZIONE OCCUPATO SU REVERSE CHANNEL OCCUPIED ON REVERSE CHANNEL	2 -
RICEVITORE RS 232-C SELEZIONATO RECEIVER SELECTION ON RS 232 - C	PON 1
TRASMETTITORE RS 232-C SELEZIONATO TRANSMITTER SELECTION ON RS 232 - C	PON 1

PONTICELLI
JUMPERS

PON - A
PON - B
PON - C
PON - D



Data	Mov.	Data	Verif.	Verif.
			<i>Est. line</i>	<i>rec</i>
			Segue sul foglio N°	1
			Codice	a
			4 2 1 5 6 4	M
				Buff

SN 75/1

PRINTED IN ITALY BY OLIVETTI MKTG/DT - IVREA

MODO DI FUNZIONAMENTO OPERATING MODE	J054 (G0092)	
TEST STAC STAC TEST	- - - -	
FREE RUNNING	4 - 17	
FULL-DUPLEX - PROCEDURA DI COLLOQUIO FULL-DUPLEX - PROCEDURE	4 - 18	
XON - XOFF (FREE - RUNNING)	4 - 18 - 19	

VARIANTI PRESTAZIONALI OPERATIONAL VARIANTS	J054 (G0092)	
INVIO BREAK ALL'ACCEN- SIONE (240 msec.) BREAK GENERATION UPON SWITCH-ON (240 msec.)	4 - 20	
TEST CONTINUO (VRP 40) CONTINUOUS TEST (VRP 40)	4 - 21	
FORZA CR DOPO MOVIMENTO CARTA (VRP 50) CARRIAGE RETURN AFTER LINE FEED (VRP 50)	4 - 22	
PONI LOCALE PER BELL (VRP 60) LOCAL SETTING FOR BELL (VRP 60)	4 - 23	
FORZA LF DOPO CR (NAZ40) LINE FEED AFTER CARRIAGE RETURN	4 - 41	

FORMATO CARATTERE CHARACTER FORMAT	J054 (G0092)	
7 bit 7 bit	4 - 8	
8 bit 8 bit	- -	
PARITA' PARI EVEN PARITY	- -	
PARITA' DISPARI ODD PARITY	4 - 10	
SENZA PARITA' WITHOUT PARITY	4 - 9	
1 bit di STOP 1 STOP bit	4 - 12	
1,5 bit di STOP 1.5 STOP bits	4 - 11	
2 bit di STOP 2 STOP bits	- -	

VELOCITA' SCAMBIO DATI DATA EXCHANGE SPEED	J054 (G0092)	
110 BpS 110 bits per second	- - -	
134,5 BpS	4 - 13 - 15 - 16	
150 BpS	4 - 16	
200 BpS	4 - 13 - 15	
300 BpS	4 - 15	
600 BpS	4 - 13 - 16	
1200 BpS	4 - 14	
1800 BpS	4 - 14 - 16	
2400 BpS	4 - 15 - 16	
4800 BpS	4 - 14 - 15	
9600 BpS	4 - 14 - 15 - 16	

TENSIONE RETE MAINS VOLTAGE	TRASFORMATORE T362 TRANSFORMER T362		
	COLLEGARE CONNECTION FASE1 FASE2 PHASE1 PHASE2	PONTICEL- LARE JUMPER	
100V - 60 Hz	1	3	4 - 8,2 - 7
115V - 60 Hz	1	5	6 - 9,2 - 7
220V - 60 Hz	1	9	6 - 7

TENSIONE RETE MAINS VOLTAGE	TRASFORMATORE T361 TRANSFORMER T361		
	COLLEGARE CONNECTION FASE1 FASE2 PHASE1 PHASE2	PONTICEL- LARE JUMPER	
100V - 50 Hz	1	3	4 - 8,2 - 7
120V - 50 Hz	1	5	6 - 9,2 - 7
200V - 50 Hz	1	8	4 - 7
220V - 50 Hz	1	8	6 - 7
240V - 50 Hz	1	9	6 - 7

olivetti Descrizione PR430 (CON ALI 254) PIASTRE : AT633 - G0092 - IF063 BOARDS		Mov.	Data	Mov.	Data	Visto	Visto
		Acc.	19-3-62				
Prodotto: XU7750				Segue sul foglio N°		N° foglio	
Fila Data 18-12-80		CARTELLINO DI SPECIALIZZAZIONE Specialization Card		Codice		a Suff	
				6 6 5 8 8 2 Z x x			

Programmazione specifica per 20/60 mA
Specific programming for 20/60 mA CURR

MODALITA' SCAMBIO DATI
DATA EXCHANGE PROCEDURES

FULL DUPLEX - PROCEDURA
DI COLLOQUIO
FULL-DUPLEX - PROCEDURE

XON - XOFF (FREE RUNNING)

N.B.: Scollegare il ponticello 34 - 35
Disconnect jumper 34 - 35 on J054

VRP30	VRP50	CALLA	SEB00	RECHO	T105A	T108A	R109A	1PR00	3NA20	VRP20	M
19	20	21	22	23	24	25	26	27	28	29	30
31	32	33	34	35	36	37	38	39	40	41	42
43	44										

● DIP SWITCHES ON

TX ATTIVO 20 mA
ACTIVE TX 20 mA

TX ATTIVO 60 mA
ACTIVE TX 60 mA

TX PASSIVO
PASSIVE TX

RX ATTIVO 20 mA
ACTIVE RX 20 mA

RX ATTIVO 60 mA
ACTIVE RX 60 mA

RX PASSIVO
PASSIVE RX

DIP SWITCHES
TS09 - TS08

MEN12	1	2	PIU12
TRADO	3	4	REDA1
SESHO	5	6	M
RXDA1	7	8	M
T111A	9	10	T
RECHO	11	12	T
T118A	13	14	T120A
T103A	15	16	T108A
T105A	17	18	R125A
R109A	19	20	R107A
R106A	21	22	R104A
T126A	23	24	R121A

A (PUNTI 4 - 3 - 44).

O NUMERO DEI PUNTI DI MAS-
LIA DI RAGGRUPPARE TRA LO-
E) PIU' SEGNALI DA COLLEGA-

(INS 4 - 3 - 44).

SMALL NUMBER OF EARTH PINS
WHICH ARE TO BE EARTHED SHOULD
BE CONNECTED.

SN 75/2

N° foglio	Codice	a	Suff
2/2	6 6 5 8 8 2	Z	x x

2.7.4 CONNECTING TO AN AC SOURCE

The power switch on the Basic Module as well as the power switch on the printer should be off. The AC mains cable exits from the rear of the Basic Module. This cable should be connected to an appropriate power outlet, AFTER HAVING VERIFIED THAT THE VOLTAGE INDICATED ON THE STICKER AT THE REAR OF THE BASIC MODULE INDICATES THE SAME VOLTAGE AS THE POWER OUTLET TO BE USED. Two wire extensions should not be used.

2.7.5 SWITCHING ON (CPU 1042)

Insert the system diskette in one of the disk drives. The power switch on the Basic Module can now be switched on. The Light Emitting Diode (LED) on the keyboard should light up. If the LED does not light one has to immediately check the power outlet. If the LED is on, after about 8 seconds the following should appear on the display:

```
-----  
M20 system configuration:  
total memory size:      XXX kbytes  
user memory size:       XXX kbytes  
display tpe:            Black and White or Color  
disk drive(s):          X ready  
LI.M20 PCOS VER. XX  
-----
```

This means that the Power Up diagnostics have run successfully. Power up diagnostics which are run automatically after switching on or after pushing the RESET button verify that enough of the M20 functions are operable to allow the running of additional diagnostic programs. If the power up diagnostics do not run to completion an error code should appear on the Display and on the printer. Refer to the power Up diagnostics chapter for a detailed account of these diagnostics.

Turning the printer on and off while the computer is in use may cause abnormal operation and the computer may 'hang up', requiring the user to reset the system. It should be pointed out to the customer that he should not switch on and off the system unnecessarily. Should something go wrong during the operation of the system, the user should first press the Control key in conjunction with the RESET key on the keyboard. If this operation has no effect the RESET button located at the right rear side of the Basic Module should be pressed.

2.7.5.1 Procedures To Be Followed When Installing Hard Disk Systems

This section describes the procedure for installing PCOS on a hard disk M20 system. This section covers both the first installation and also updating the hard disk drive with a new version of PCOS.

The first thing to do is format the hard disk drive. To format the hard disk drive you must first load PCOS from the diskette you received with the system. Do this by inserting the PCOS system diskette in the floppy disk drive and turning on power to the system. Press the "f" key on the keyboard before the two beeps are heard. This causes the Bootstrap ROM to load PCOS from the floppy disk rather than from the hard disk. This is necessary because there may be older versions of PCOS or test programs remaining on the hard disk drive from the Manufacturing Test process.

After PCOS is loaded type "vf 10:". This tells PCOS to run the Vformat program and to format the hard disk drive (drive 10). Vformat will tell you each cylinder on the hard disk that is being formatted.

When the Vformat program is complete (as signified by the message Formatting Complete), the next step is to put a bootstrap file on the hard disk. Do this by typing "ps 10:". This invokes the Psave utility to install the current version of PCOS on the hard disk drive. When the Psave utility is complete it will automatically re-boot the PCOS on the hard disk.

The next step is to copy all the PCOS commands to the hard disk drive. This is done by using the PCOS Fcopy command. To copy all the floppy disk files to the hard disk type "fc 0:* 10:". The Fcopy will copy all of the files from the floppy diskette to the hard disk. Below is a flowchart illustrating this procedure.

! Insert PCOS disk in mini-floppy!

!
!

! Switch on M20 System !

!
!
!
!

! Press "f" key on the keyboard !
! before the two beeps are !
! heard !

!
!
!

! Type in vf 10: !

!
!
!

! Message: Formatting Complete !
! appears if formatting was !
! was successful !

!
!
!

! Type in ps 10: !

!
!
!

! Type in fc 0:* 10: !

!
!
!

-----Question "Do you want
to overwrite PCOS.SAV
(y,n)?"
Type "n".

! INSTALLATION COMPLETE !

UPDATE INSTALLATION

If the hard disk drive has been through the initial installation (as described above), and all that is required is to place the latest version of PCOS and the utilities on the hard disk, the following procedure should be used. Boot the hard disk system and then place the new PCOS diskette in the floppy disk drive. Type "fc %f 0:* 10:" which will invoke the Fcopy utility to copy all the files from the floppy diskette to the hard disk. The "%f" (force) option will cause Fcopy to copy the files to the hard disk even though the files may already exist on the hard disk.

NOTE: THIS PROCEDURE DOES NOT CALL FOR FORMATTING THE HARD DISK AND THEREFORE WILL NOT HARM OTHER FILES THAT MAY BE PRESENT ON THE HARD DISK.

2.8 UPGRADES

This section deals with the upgrades made in the field on the M20 system. The first upgrades or installations described include:

- memory upgrade
- IEEE 488 Interface Board installation
- Second mini-floppy disk drive installation
- Twin RS 232C Interface Board installation
- APB 1086 Board installation
- Colour Display Installation

2.8.1 MEMORY UPGRADE

Materials required:

Memory Expansion Board

The memory board to be installed (whether 32KB or 128KB type) plugs into slot J10 on the motherboard, that is the slot nearest the front of the Basic Module. The first thing to do is remove the Basic Module cover. This is done by untightening the two screws at the rear of the Basic Module and then lifting the rear of the cover. Ensure jumper X2-7 on the motherboard is open. See jumper chart tables at end of this section.

In order to install the memory board, plug it into slot J10 with the com-

ponent side facing the front of the machine.

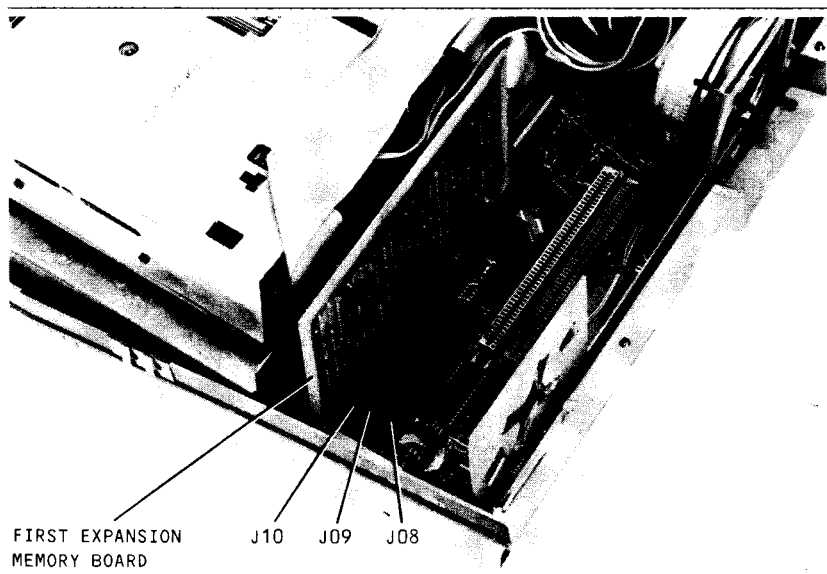


Fig. 2-4 Installation of memory expansion board

One can also install a second or third plug in memory board. The procedure is the same except that the second plug in board plugs into connector J9 and the third plug in board plugs into connector J8. Finally, reinstall the Basic Module cover.

NOTE: ONE CAN ONLY INSTALL MEMORY BOARDS OF THE SAME TYPE i.e. one cannot mix 32KB type boards and 128KB type boards.

CONFIGURATION	Z1-Z2	K1-K2	E1-E2	V1-V2	W1-W2	M1-M2	X1 - X8	X2 - X7	X3 - X6	U62/3/4/5	U86 A
M 20 WITH OUT ANY EXPANSION BOARDS	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	ON	OFF	ICs PRESENT	OFF
M 20 WITH AT LEAST ONE B/W 32KB EXPANSION BOARD	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	OFF	OFF	ICs PRESENT	OFF
M 20 WITH AT LEAST ONE B/W 128KB EXPANSION BOARD	Z - Z1	K - K1	E - E1	V - V2	W - W1	M - M2	ON	OFF	OFF	ICs NOT PRESENT	ON
M 20 WITH ONE 32KB COLOUR BOARD (4 COLOURS)	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	OFF	ON	ICs PRESENT	OFF
M 20 WITH ONE 128KB COLOUR BOARD (4 COLOURS)	Z - Z1	K - K1	E - E1	V - V2	W - W1	M - M2	OFF	ON	ON	ICs NOT PRESENT	ON
M 20 WITH TWO 32KB COLOUR BOARDS (8 COLOURS)	Z - Z1	K - K2	E - E2	V - V1	W - W2	M - M1	ON	OFF	ON	ICs PRESENT	OFF
M 20 WITH TWO 128KB COLOUR BOARDS (8 COLOURS)	Z - Z1	K - K1	E - E2	V - V2	W - W1	M - M2	ON	ON	ON	ICs NOT PRESENT	ON

2.8.2 IEEE 488 INTERFACE

Materials required:

IEEE 488 Interface Board

Signal ribbon cable which connects board to rear of Basic Module

IEEE Peripheral Cable

The IEEE 488 interface board plugs into slot J3 or J4 on the motherboard. The first thing to do is to remove the Basic Module cover. This is done by first untightening the two screws at the back of the Basic Module cover and then lifting the rear of the cover.

In order to install the IEEE 488 interface board, plug it into slot J3 or J4 on the motherboard with the component side facing the front of the machine. A flat ribbon cable plugs into the connector J1 on the IEEE board. The other end of the flat cable has a connector which has to be screwed to the back of the Basic Module cover. Peripherals are connected to the M20 by means of a cable (PIC1037) which plugs into the connector at the back of the Basic Module cover.

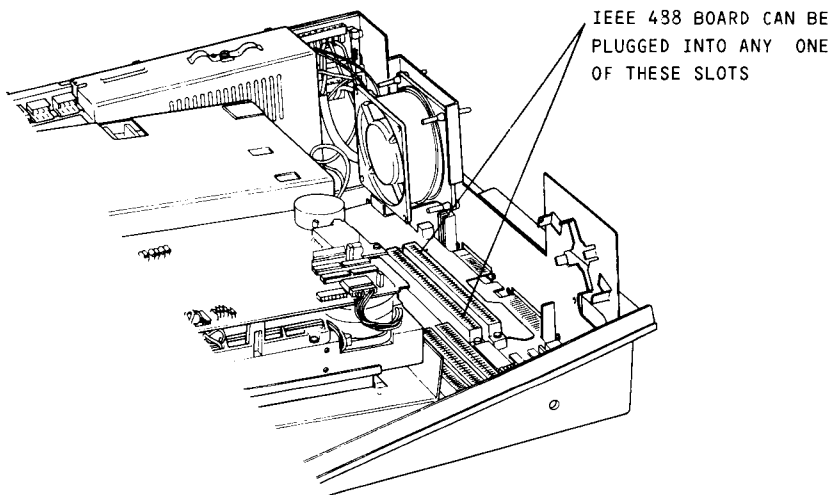


Fig. 2-5 Installation of IEEE board

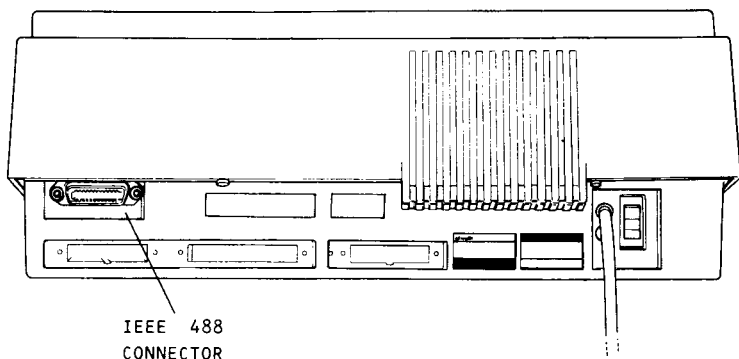


Fig. 2-6 IEEE 488 connector at rear of Basic Module

2.8.3 INSTALLATION OF SECOND MINI-FLOPPY DISK DRIVE

Materials Required:

Mini-Floppy Disk Drive

Signal Ribbon Cable (with three connectors)

Power Cable

Terminator Resistor (preferably 330 ohm)

NOTE: The right hand disk drive in this manual is drive 0, while the left hand one is drive 1. In other manuals (Mini-Floppy General Service Manual) the numbering may be different.

The following steps should be followed when installing a second disk drive:

- 1) Remove the Basic Module cover by loosening the two screws at the rear of the Basic Module and then lifting the rear of the cover.
- 2) Remove the ribbon connector from J2 on the motherboard and from J1 on the disk drive PCB.
- 3) Remove the power connector from the disk drive connector J2. J2 is the disk drive DC power connector and is located near the spindle drive motor and mounted on the component side of the disk drive PCB.

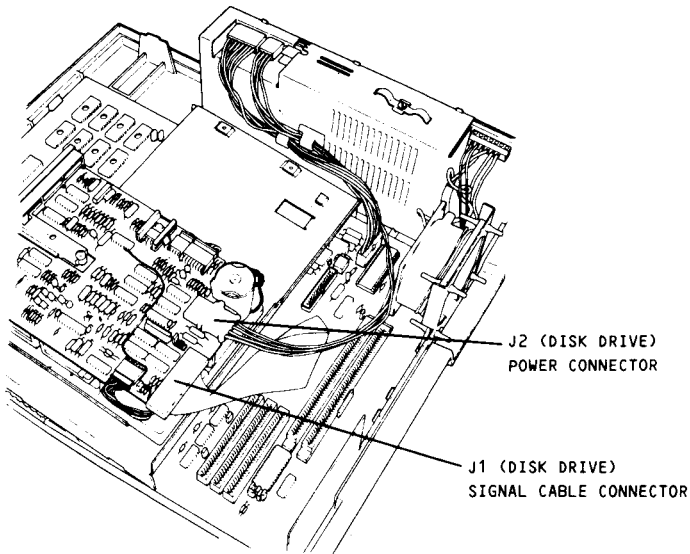


Fig. 2-7 M20 with one Mini-Floppy Disk drive

4) Remove the whole metal base of the mini-floppy disk drive by first sliding the base slightly forward and then lifting the base from the Basic Module.

5) Remove the metal cover of the original disk drive by loosening the two screws on each side. This original disk drive is identified as disk drive number 0. Ensure that this disk drive is jumpered for disk drive number 0. Refer to the Mini-Floppy General Service Manual for further details. THE TERMINATOR RESISTORS MUST BE PRESENT IN ALL THE UNITS OF THE DAISY CHAIN.
Replace the metal cover.

6) Remove the metal cover of the disk drive to be installed by loosening the two screws on each side. Ensure that this disk drive is jumpered for drive number 1 and the supply voltage jumpers are correctly fitted. The M20 provides the mini-floppy disk drive with +12VDC ON TWO LEADS. Refer to the General Service Manual of the Mini-Floppy Disk Drive. THE TERMINATOR RESISTORS MUST BE PRESENT IN ALL THE UNITS OF THE DAISY CHAIN. N.B. THERE ARE TWO TYPES OF TERMINATOR RESISTORS - 150 OHM ONES AND 330 OHM ONES. IF 150 OHM ONES ARE USED, PLEASE REFER TO THE FOLLOWING TABLE:

BOARD AT064

DRIVE 0: 150 ohm terminator (only pins 1 and 4 inserted)

DRIVE 1: 150 ohm terminator inserted

BOARD AT109

DRIVE 0: 150 ohm terminator (only pins 1 and 5 inserted)

DRIVE 1: 150 ohm terminator inserted

Pin 1 is marked with a small dot.

7) Place the new disk firmly on the metal base. Tighten the screw at the front.

8) Place the whole metal base with the two mini-floppy disk drives mounted on it back again in the Basic Module. There are 6 grooves on the bottom of the Basic Module in order to ensure that the whole metal base is properly seated.

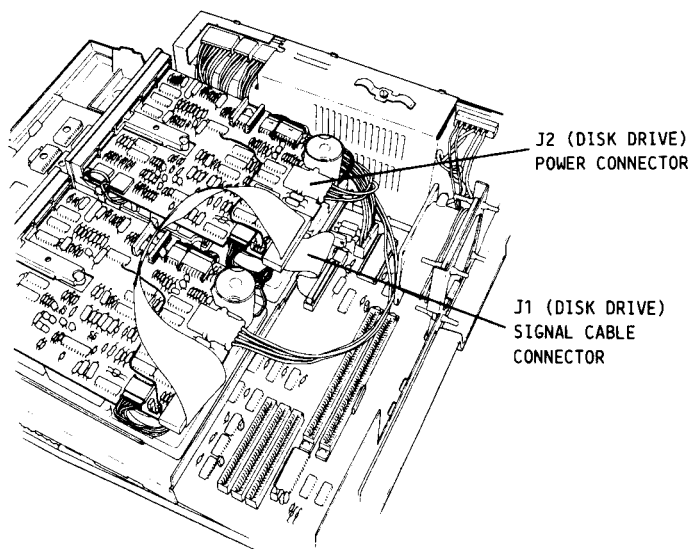


Fig. 2-8 M20 with two Mini-Floppy Disk Drives

9) Connect the power cable to drive 0. This power cable from connector J061 on the power supply in the Basic Module plugs into the DC power connector J2 on disk drive 0. J2 is located near the spindle drive motor and is mounted on the component side of the PCB on the disk drive.

10) Connect power cable to disk drive 1. This power cable from connector J061 on the power supply in the Basic Module plugs into the DC power connector J2 on disk drive number 1. J2 is located near the spindle drive motor and is mounted on the component side of the PCB on disk drive number 1. Note that the two connectors on the power supply nearest the potentiometer

are both J061 and both provide identical DC voltages to the disk drives.

11) Connect the signal cable to the disk drives. The signal cable has three connectors: the first one fits into connector J2 on the motherboard, the second one fits into connector J1 on the disk drive 0, the third one fits into connector J1 of disk drive 1. Ensure that the cable connector that fits into the disk drive number 1 is oriented so that the cable exits from the bottom.

12) Install the new front cover of the disk drives.

13) Replace the Basic Module cover.

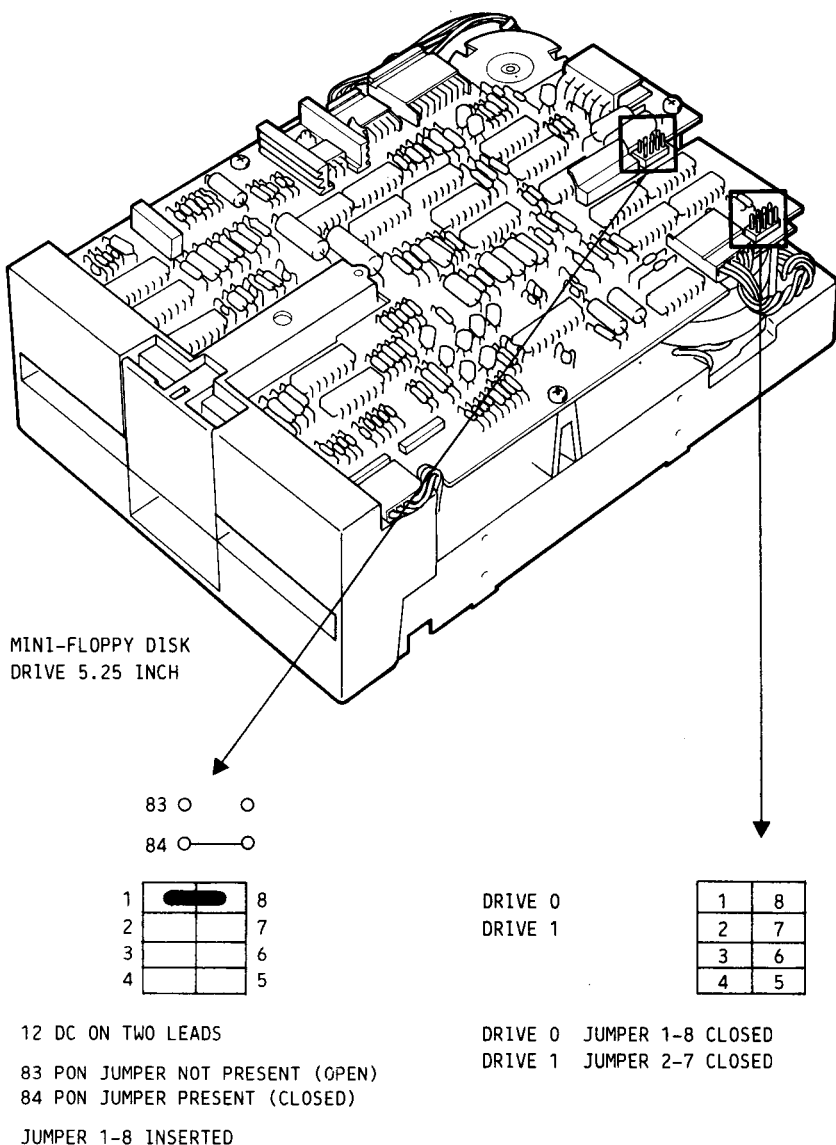


Fig. 2-9 Setting of electronic board AT064

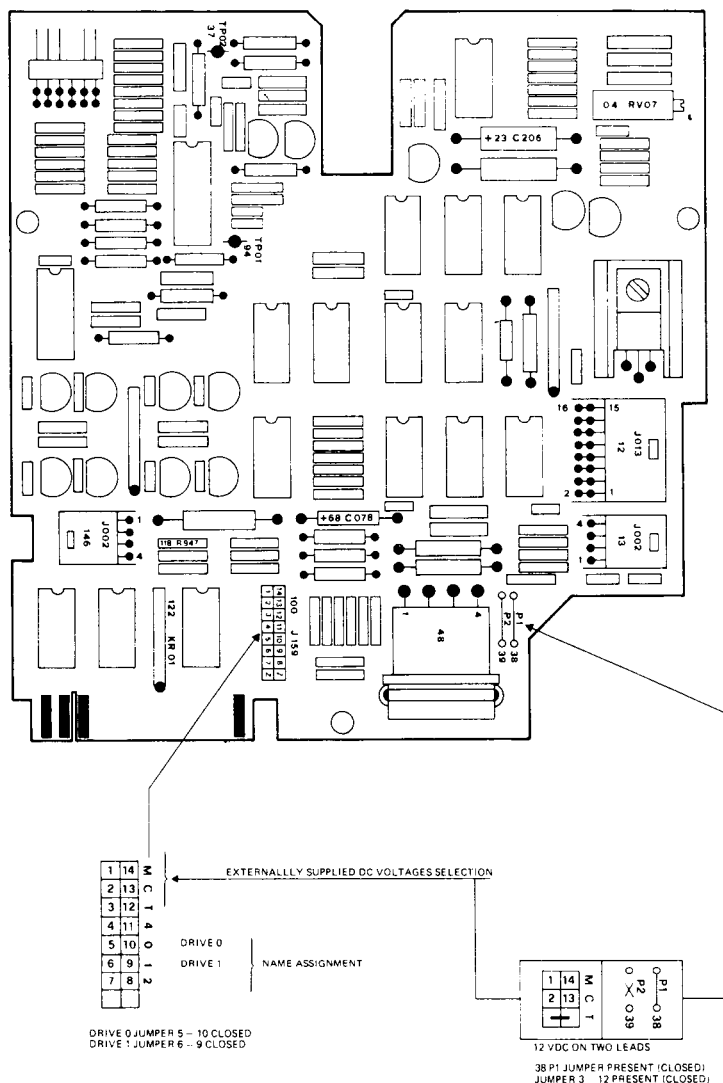


Fig. 2-10 Setting of electronic board AT109

2.8.4 TWIN RS 232C INTERFACE BOARD

Materials Required:

Twin RS 232C Board

Flat ribbon cable

Card Edge Connector

Cable to connect peripheral (s)

The Twin RS 232C board plugs into either slot J3 or J4 on the motherboard. The first thing to do is remove the Basic Module cover. This is done by untightening the two screws at the back of the Basic Module cover and then lifting the rear of the cover. In order to install the Twin RS232C interface board, plug it into slot J3 or J4 on the motherboard with its component side facing the front of the machine. Consult the jumper charts section for the exact location and function of all the jumpers present on this board.

A 40 flat ribbon cable connects the Twin RS232C board to a small card edge PCB which is fixed to the rear of the Basic Module cover by two screws. The peripheral cable then plugs into this card edge PCB. There are three different types of cables to be used depending on the type of peripherals connected.

Cable 1 (CAV030) - for 2 peripherals using both RS 232C interfaces

Cable 2 (CAV031) - for 2 peripherals using both current loop interfaces

Cable 3 (CAV029) - for 2 peripherals, one using RS 232C interface, the other using current loop interface.

Cable 4 (CAV032) - General Purpose Cable

The current loop section of the cable is composed of 4 bare wires which have the following colours:

White - TCL01 (transmit current loop channel 1)

White/Red - TCL02 (transmit current loop channel 2)

White/Black - RCL01 (receive current loop channel 1)

White/Brown - RCL02 (receive current loop channel 2)

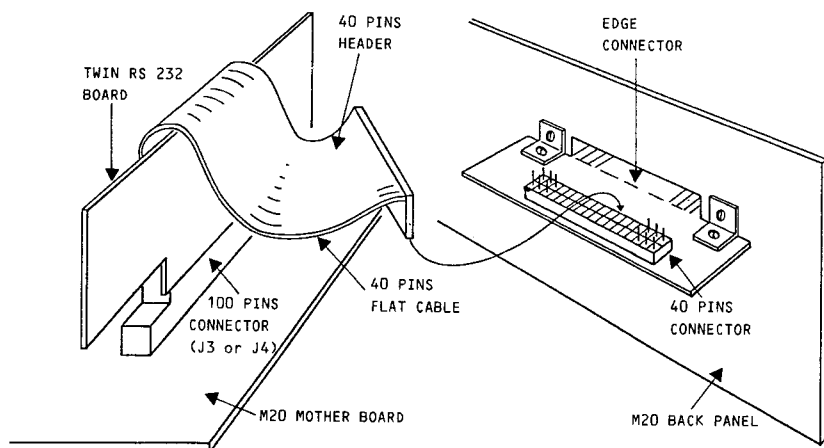


Fig. 2-11 Installation of Twin RS232 C board

2.8.4.1 Jumpers

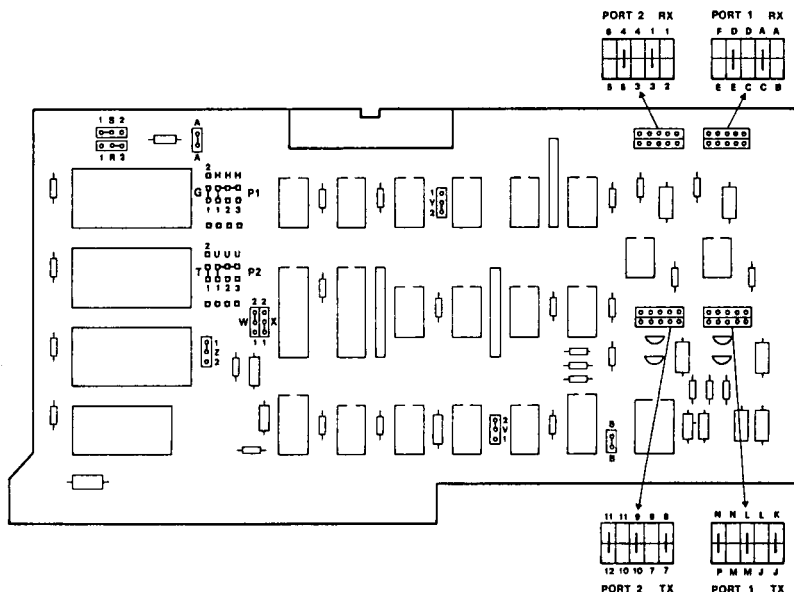


Fig. 2-12 Twin RS232C Interface Board

The TWIN RS 232C Board is jumpered by Production to work in the following manner:

Both Channels:

RS 232C with internal transmission clock, with external receive clock, with DSR and DTS active, in synchronous mode.

Jumpers always closed:

A-A, B-B, A-C, D-E, J-K, M-L, P-N, 1-G, 1-H, 1-S, 1-T, 1-U, 1-Z, 1-X, 2-R, 2-V, 2-W, 2-Y, 1-3, 4-5, 7-8, 9-10, 11-12.

2.8.5 INSTALLATION OF APB 1086 BOARD

Materials Required:

APB 1086 Board

Anti-disturbance shield (if no other board is plugged into J3 or J4)

In order to install the APB 1086 (G0246) the following steps are necessary:

- 1) Remove the M20 Basic Module cover.
- 2) Remove the keyboard and the mini-floppy disk unit assembly.
- 3) Check the motherboard release level.
- To upgrade systems with level 'D' motherboards the procedure is shown in the table below:

! POSITION !	REMOVE	! INSTALL !
! U 1 !	! EPROM PA 61 1.0 !	! EPROM PA77 2.0!
! !	! H1ST !	! H1ST !
! !	! code: 335596P !	! code: 336297U !
! U 16 !	! EPROM PA 62 1.0 !	! EPROM PA78 2.0!
! !	! L1ST !	! L1ST !
! !	! code: 335597Q !	! code: 336298D !
! ZA !	! Jumper ZA-2 !	! Jumper ZA-1 !

- To upgrade systems with level 'CP' motherboards consult the following publication: BIT code 3874277X15

- 4) Reinstall the keyboard and the mini-floppy disk unit assembly.
- 5) Insert the anti-disturbance shield (code 336174 Y) as shown at point A

in the figure below.

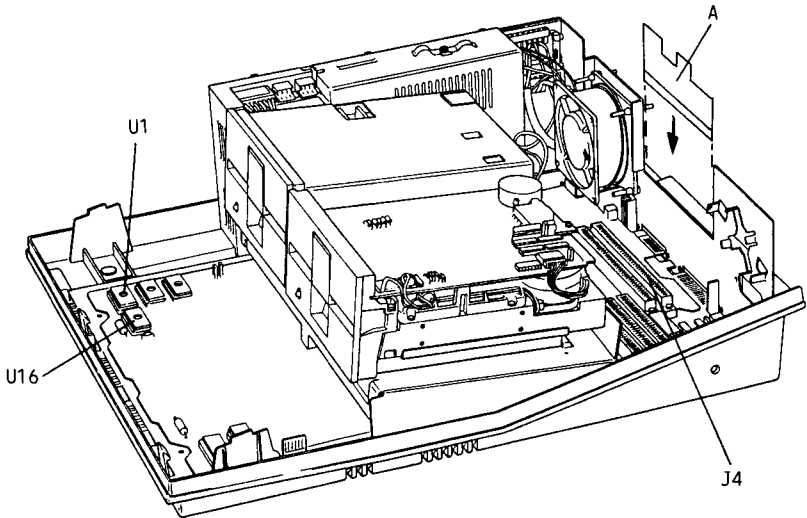


Fig. 2-13 Installation of the APB 1086

6) Insert the APB 1086 (G0246) in the motherboard slot J4 as shown in the figure above.

7) Reinstall the M20 Basic Module cover.

2.8.6 INSTALLATION OF COLOUR DISPLAY

Materials Required:

Colour Display

Power Cable

Signal Cable

Two Colour Memory Expansion Boards (for 8 colour systems)

One Colour Memory Expansion Board

Board MI204

The procedure for installing the Colour Display is as follows:

1) Install the Board MI204 in location U57 on the motherboard.

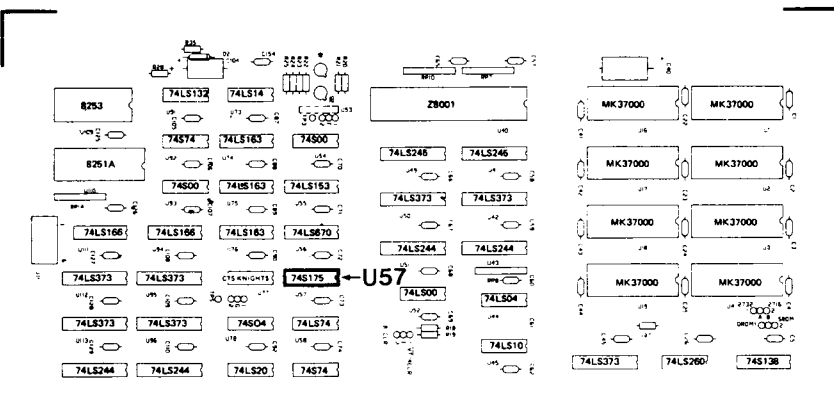


Fig. 2-14 Motherboard Component view

2) Install the jumpers on the motherboard according to whether a 128KB or a 32KB colour board is going to be installed.

32KB(4 Colour)	32KB(8 colour)	128K(4 colour)	128KB(8 colour)
Z-Z1	Z-Z1	Z-Z1	Z-Z1
K-K2	K-K2	K-K1	K-K2
E-E1	E-E2	E-E1	E-E2
V-V1	V-V1	V-V2	V-V2
W-W2	W-W2	W-W1	W-W1
M-M1	M-M1	M-M2	M-M2
X1-X8 OFF	X1-X8 ON	X1-X8 OFF	X1-X8 ON
X2-X7 OFF	X2-X7 OFF	X2-X7 ON	X2-X7 ON
X3-X6 ON	X3-X6 ON	X3-X6 ON	X3-X6 ON
U62/3/4/5 ON	U62/3/4/5 ON	U62/3/4/5 OFF	U62/3/4/5 OFF
U86A OFF	U86A OFF	U86A ON	U86A ON

3) Connect the Power Cable to the M20 Supply

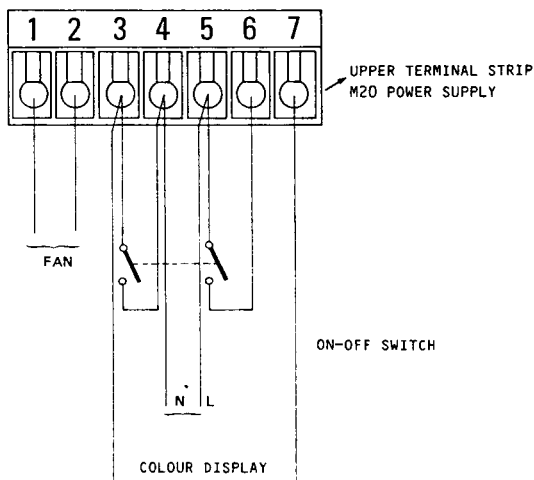


Fig. 2-15 Connection of Video Power Cable to M20

4) Connect the signal and power cables to the colour video as explained in section 2.7.2.

2.9 JUMPER CHARTS

This section deals with the jumpers on the following modules or boards:

- Keyboard
- Power Supply
- 32KB Memory Expansion Board
- IEEE 488 Interface Board
- Twin RS 232C Interface Board
- Motherboard 'CP' level with 1.0 Bootstrap ROM
- Motherboard 'D' level with 1.0 Bootstrap ROM
- Motherboard (all levels) with 2.0 Bootstrap ROM

2.9.1 KEYBOARD

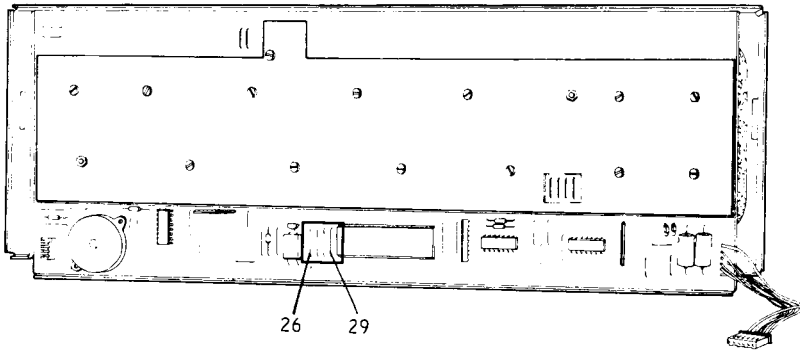


Fig. 2-16 Keyboard

Keyboard jumper 26 is the jumper nearest the quartz oscillator and 29 the

jumper nearest the keyboard processor.

KEYBOARD					
COUNTRY	JUMPERS				
	29	28	27	26	
ITALY	X	X	X	X	
W. GERMANY	X	X	X		
FRANCE	X	X		X	
U.K.	X	X			
USA ASCII BASIC	X		X	X	
SPAIN	X		X		
PORTUGAL	X			X	
SWEDEN/FINLAND	X				
DENMARK		X	X	X	
KATAKANA		X	X		
NORWAY		X			
SWITZERLAND - F			X		
SWITZERLAND - D				X	
X = CLOSED					

Fig. 2-17 Keyboard Jumpers table

2.9.2 POWER SUPPLY

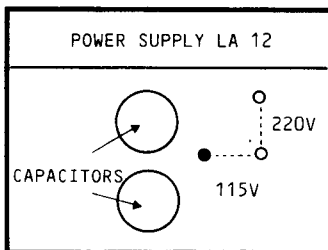


Fig. 2-18 Power Supply Jumpers

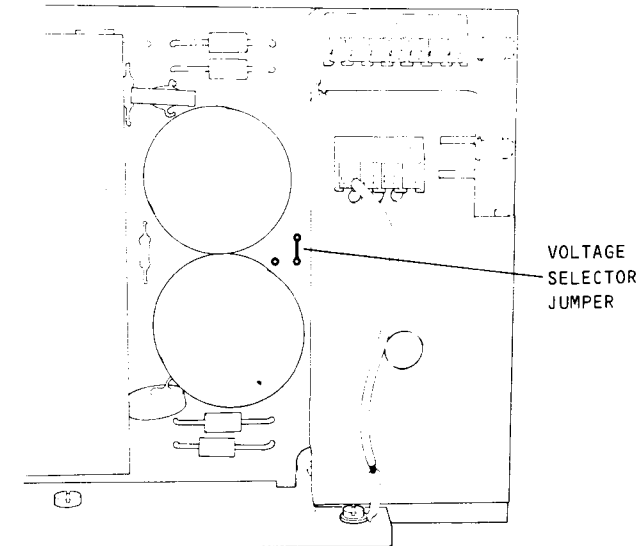


Fig. 2-19 Power Supply

2.9.3 32KB MEMORY EXPANSION BOARD

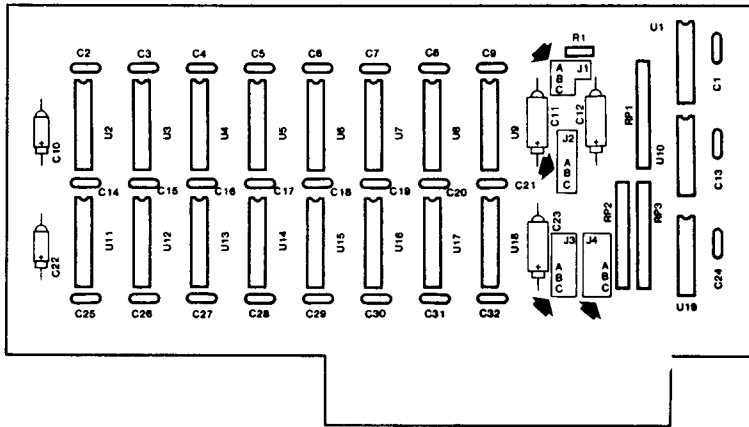


Fig. 2-20 32KB Memory Expansion Board

Only the older versions of the 32KB expansion boards have jumpers. The newer versions have no jumpers. The 128KB expansion boards have no jumpers.

! J1 B-C	! Always closed (ON)!
! J2 A-B	! Always closed (ON)!
! J3 A-B	! Always closed (ON)!
! J4 B-C	! Always closed (ON)!

2.9.4 IEEE 488 INTERFACE BOARD

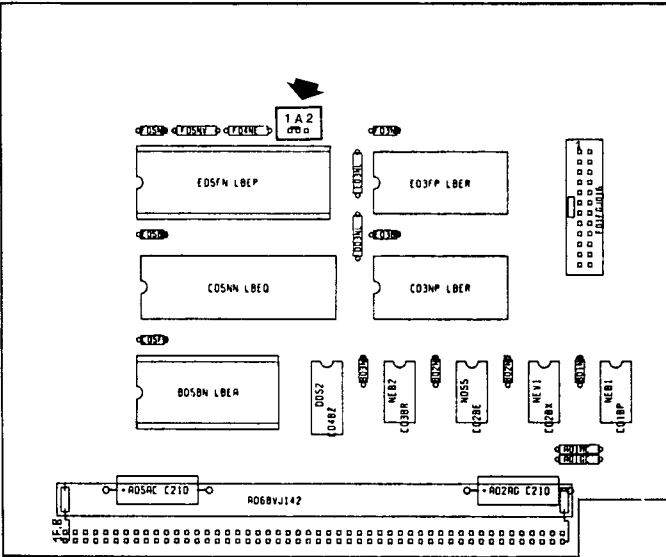


Fig. 2-21 IEEE 488 Interface Board

JUMPER	FUNCTION	NORMAL POSITION
A - 1	System Controller	Closed
A - 2	Talker/Listener	Open

Jumper A - 1 should always be closed to indicate that the M20 is the controller.

2.9.5 TWIN INTERFACE BOARD

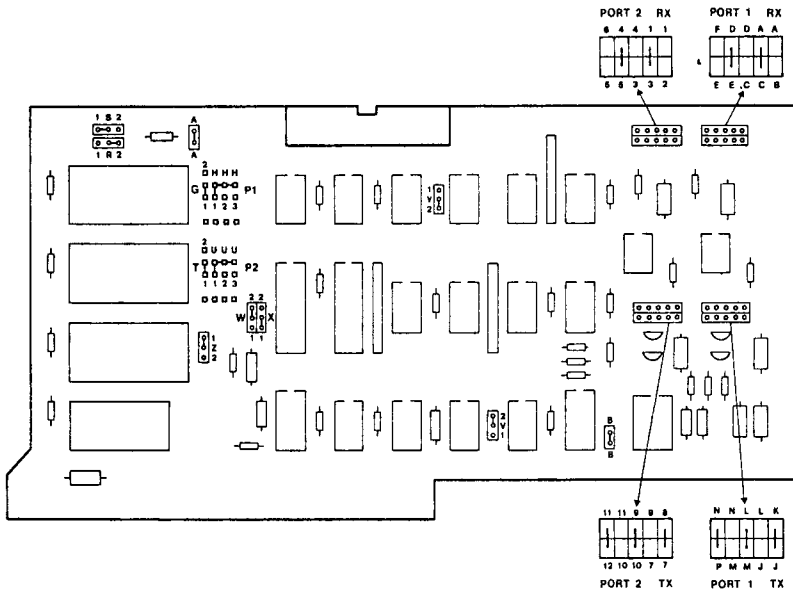


Fig. 2-22 Twin RS 232C Interface Board

RS 232C Transmission

ASYNCHRONOUS MODE:

Port 1

- B----B (Clock for 16MHz Crystal)
- 1----G (Port 1 CTS Active)
- 1----H (Port 1 DSR Active)
- 2----R (Internal Transmit Clock for Port 1)
- 2----S (Internal Receive Clock for Port 1)
- 1----Z (IR4, pin 22 of Interrupt Controller Grounded)

Port 2

- A----A (Reset Signal to Port 2)
- B----B (CLK for 16MHz Crystal)
- 1----T (Port 2 CTS Active)
- 1----U (Port 2 DSR Active)
- 2----X (Internal receive Clock for Port 2)
- 2----W (Internal Transmit Clock for Port 2)

1-----Z (IR4, pin 22 of Interrupt Controller Grounded)

SYNCHRONOUS MODE

Port 1

B-----B (CLK for 16MHz Crystal)

1-----G (Port 1 CTS Active)

1-----H (Port 1 DSR Active)

1-----S (External Receive Clock for Port 1)

1-----Z (IR4 pin 22 of Interrupt Controller Grounded)

```
!
!
!
!-----:  INTERNAL TRANSMIT CLOCK
!          2-----R (Internal Transmit Clock for Port 1)
!          2-----V (Transmit Clock 1 to outside)
!
!
!
!
!-----:  EXTERNAL TRANSMIT CLOCK
!          1-----R (External Transmit Clock for Port 1)
```

Port 2

A-----A (Reset Signal to Port 2)

B-----B (CLK for 16 MHz Crystal)

1-----T (Port 2 CTS Active)

1-----U (Port 2 DSR Active)

1-----X (External Receive Clock for Port 2)

1-----Z (IR4, pin 22 of Interrupt Controller Grounded)

```
!
!
!
!-----:  INTERNAL TRANSMIT CLOCK
!          2-----W (Internal Transmit Clock for Port 2)
!          2-----Y (Transmit Clock 2 to outside)
!
!
!
!
!-----:  EXTERNAL TRANSMIT CLOCK
!          1-----W (External Transmit Clock for port 2)
```

Current Loop

Port 1

Transmit Active

B-----B (CLK for 16 MHz Crystal)
1-----G (Port 1 CTS Active)
3-----H (Port 1 DSR Grounded)
2-----S (Internal Receive Clock for Port 1)
2-----R (Internal Transmit Clock for Port 1)
1-----Z (IR4, pin 22 of the Interrupt Controller Grounded)
J-----K (TCL01, Sourcing Current, Active)
L-----M (TCL01, Sourcing Current, Active)
N-----P (TCL01, Sourcing Current, Active)

Transmit Passive

B-----B (CLK for 16 MHz Crystal)
1-----G (Port 1 CTS Active)
3-----H (Port 1 DSR Active)
2-----S (Internal Receive Clock for Port 1)
2-----R (Internal Transmit Clock for Port 1)
1-----Z (IR4, pin 22 of the Interrupt Controller Grounded)
J-----L (TCL01, NOT Sourcing Current, Passive)
M-----N (TCL01, NOT Sourcing Current, Passive)

Receive Active

B-----B (CLK for 16 MHz Crystal)
1-----G (Port 1 CTS Active)
3-----H (Port 1 DSR Grounded)
1-----Z (IR4, pin 22 of Interrupt Controller Grounded)
2-----S (Internal Receive Clock for Port 1)
2-----R (Internal Transmit Clock for Port 1)
A-----B (RCL01, Sourcing Current, Active)
D-----C (RCL01, Sourcing Current, Active)
E-----F (RCL01, Sourcing Current, Active)

Receive Passive

B-----B (CLK for 16 MHz Crystal)
1-----G (Port 1 CTS Active)
3-----H (Port 1 DSR Grounded)
2-----S (Internal Receive Clock for Port 1)
2-----R (Internal Transmit Clock for Port 1)
1-----Z (IR4, pin 22 of Interrupt Controller Grounded)
A-----C (RCL01, NOT Sourcing Current, Passive)
D-----E (RCL01, NOT Sourcing Current, Passive)

PORT 2

Transmit Active

B-----B (CLK for 16 Mhz Crystal)
 A-----A (Reset Signal to Port 2)
 1-----Z (IR4, pin 22 of Interrupt Controller Grounded)
 2-----T (Port 2 CTS Grounded)
 3-----U (Port 2 DSR Grounded)
 2-----W (Internal Transmit Clock for Port 2)
 2-----X (Internal Receive Clock for Port 2)
 7-----8 (TCL03, Sourcing Current, Active)
 9-----10 (TCL03, Sourcing Current, Active)
 11---12 (TCL03, Sourcing Current, Active)

Transmit Passive

B-----B (CLK for 16 MHz Crystal)
 A-----A (Reset Signal for Port 2)
 1-----Z (IR4 pin 22 of Interrupt Controller Grounded)
 2-----T (Port 2 CTS grounded)
 3-----U (Port 2 DSR grounded)
 2-----W (Internal Transmit Clock for Port 2)
 2-----X (Internal Receive Clock for Port 2)
 7-----9 (TCL03 NOT Sourcing Current, Passive)
 10---11 (TCL03 NOT Sourcing Current, Passive)

Receive Active

B-----B (CLK for 16 MHz Crystal)
 A-----A (Reset signal to port 2)
 1-----Z (IR4 pin 22 of Interrupt Controller Grounded)
 2-----T (Port 2 CTS Grounded)
 3-----U (Port 2 DSR Grounded)
 2-----W (Internal Transmit Clock for Port 2)
 2-----X (Internal Receive Clock for Port 2)
 1-----2 (RCL03, Sourcing Current, Active)
 3-----4 (RCL03, Sourcing Current, Active)
 5-----6 (RCL03, Sourcing Current, Active)

Receive passive

B-----B (CLK for 16 MHz Crystal)
 A-----A (Reset signal to port 2)
 1-----Z (IR4 pin 22 of Interrupt controller grounded)
 2-----T (Port 2 CTS Grounded)
 3-----U (Port 2 DSR Grounded)
 2-----W (Internal Transmit Clock for port 2)
 2-----X (Internal Receive Clock for port 2)
 1-----3 (RCL03 NOT Sourcing Current, Passive)
 4-----5 (RCL03 NOT Sourcing Current, Passive)

Other jumpers:

2-----V (Transmit Clock 1 to outside)
 1-----V (P6629 Compatible ON/OFF signal)
 2-----Y (Transmit Clock 2 to outside)
 1-----Y (P6629 Compatible ON/OFF Signal)
 H-----2 (P6629 Compatibility - Logic Inverted)
 2-----Z (Real Time Clock -vectored)

JUMPER SETTINGS FOR TWIN RS 232C BOARD

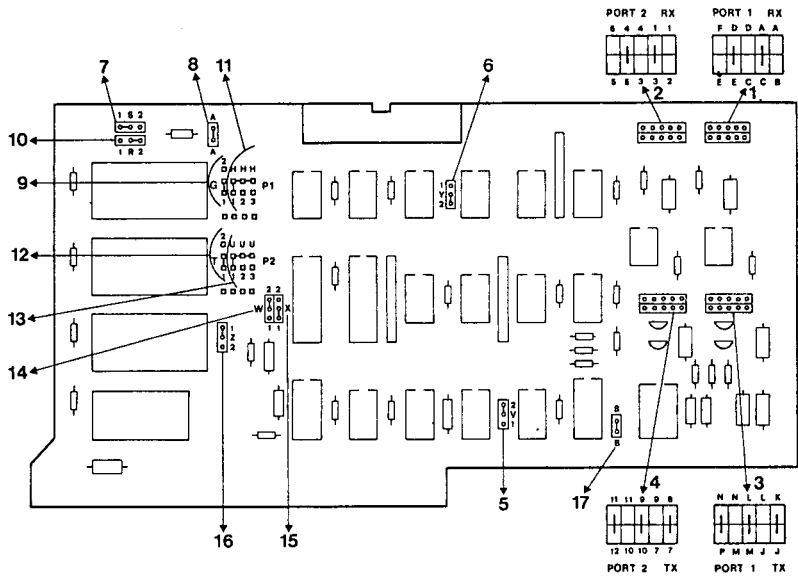


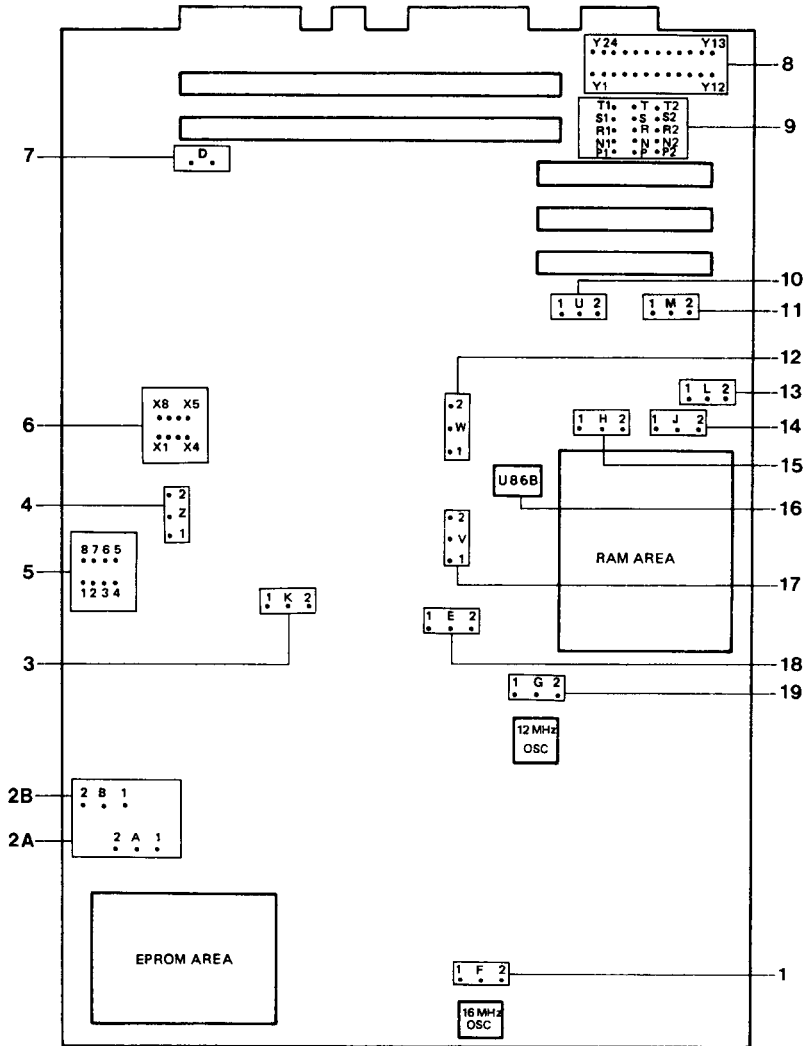
Fig. 2-23 Twin RS 232C Board

REFERENCE	JUMPER	FUNCTION	-OR I = CLOSED BY PRODUCTION
1	A - B	Port 1 Receive Side : RCLO1 Sourcing Current (Active)	
	A - C	Port 1 Receive Side : RCLO1 NOT Sourcing Current (Passive)	
	D - C	Port 1 Receive Side : RCLO1 Sourcing Current (Active)	
	D - E	Port 1 Receive Side : RCLO1 NOT Sourcing Current (Passive)	
	F - E	Port 1 Receive Side : RCLO1 Sourcing Current (Active)	
2	1 - 2	Port 2 Receive Side : RCLO3 Sourcing Current (Active)	
	1 - 3	Port 2 Receive Side : RCLO3 NOT Sourcing Current (Passive)	
	4 - 3	Port 2 Receive Side : RCLO3 Sourcing Current (Active)	
	4 - 5	Port 2 Receive Side : RCLO3 NOT Sourcing Current (Passive)	
	6 - 5	Port 2 Receive Side : RCLO3 Sourcing Current (Active)	
3	K - J	Port 1 Transmit Side : TCL01 Sourcing Current (Active)	
	L - J	Port 1 Transmit Side : TCL01 NOT Sourcing Current (Passive)	
	L - M	Port 1 Transmit Side : TCL01 Sourcing Current (Active)	
	N - M	Port 1 Transmit Side : TCL01 NOT Sourcing Current (Passive)	
	N - P	Port 1 Transmit Side : TCL01 Sourcing Current (Active)	
4	8 - 7	Port 2 Transmit Side : TCL03 Sourcing Current (Active)	
	9 - 7	Port 2 Transmit Side : TCL03 NOT Sourcing Current (Passive)	
	9 - 10	Port 2 Transmit Side : TCL03 Sourcing Current (Active)	
	11- 10	Port 2 Transmit Side : TCL03 NOT Sourcing Current (Passive)	
	11- 12	Port 2 Transmit Side : TCL03 Sourcing Current (Active)	

5	2 - V 1 - V	Transmit CLOCK 1 to Outside P6629 Compatible ON/OFF Signal	
6	2 - Y 1 - Y	Transmit CLOCK 2 to Outside P6629 Compatible ON/OFF Signal	
7	2 - S 1 - S	Internal Receive Clock for Port 1 External Receive Clock for Port 1	
8	A - A	Reset Signal to Port 2	
9	2 - G 1 - G	Port 1 CTS Grounded Port 1 CTS Active	
10	2 - R 1 - R	Internal Transmit Clock for Port 1 External Transmit Clock for Port 1	
11	H - 1 H - 2 H - 3	Port 1 DSR Active P6629 Compatibility Port 1 DSR Grounded	
12	1 - T 2 - T	Port 2 CTS Active Port 2 CTS Grounded	
13	U - 1 U - 2 U - 3	Port 2 DSR Active P6629 Compatibility Port 2 DSR Grounded	
14	2 - W 1 - W	Internal Transmit Clock for Port 2 External Transmit Clock for Port 2	
15	1 - X 2 - X	Internal Receive Clock for Port 2 External Receive Clock for Port 2	

16	1 - Z 1 - Z	Real Time Clock (Vectored) IRQ (Pin 22) of the Interrupt Controller Grounded	
17	B - B	Clk for 16 MHz Cristal	

2.9.6 LEVEL CP MOTHERBOARD



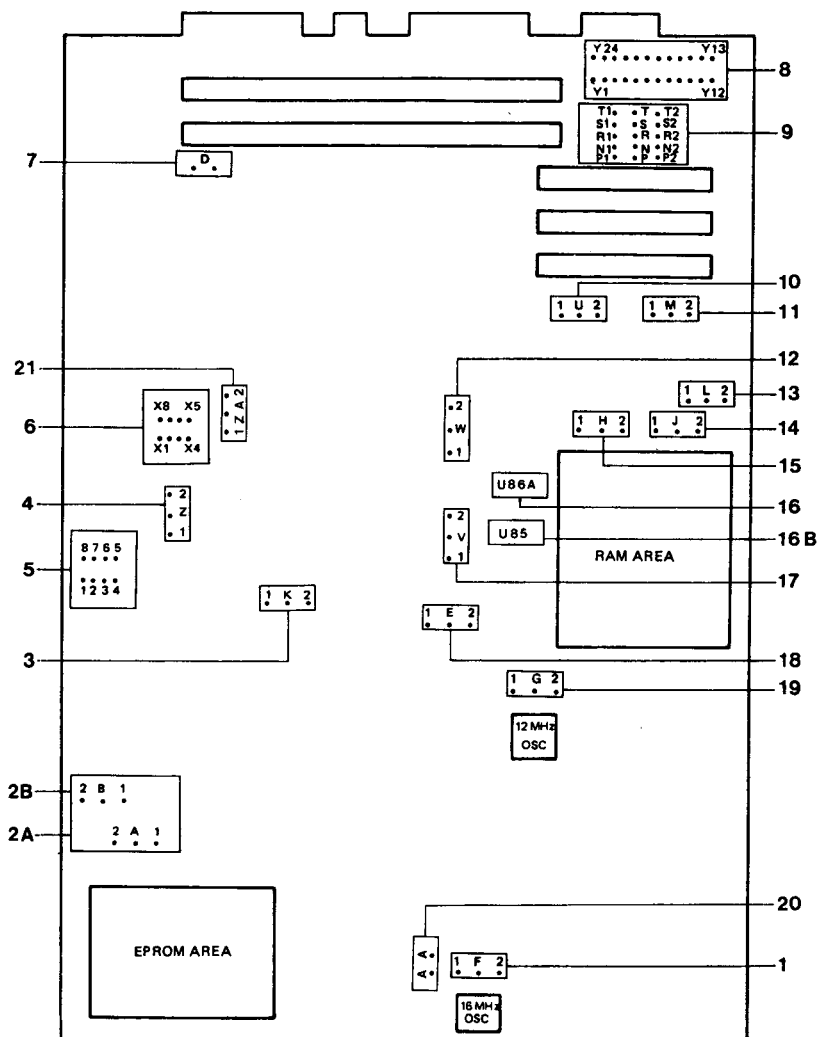
REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
1	12/12	F - F1 F - F2	Internal 16 MHz clock External clock	F - F1	F1 F F2 → .
2A	7/12	A - A1 A - A2	ROM 2732, 2764, MK 3700 ROM 2716	A - A1	A1 A A2 → .
2B	7/12	B - B1 B - B2	Dynamic ROM MK 3700 Static ROM/EPROM	B - B2	B1 B B2 . →
3	2/12	K - 1 K - 2	512 KB System 128 - 224 KB System	K - 2	1 K 2 . →
4	10/12	Z - Z1 Z - Z2	M20 with or without memory exposition board Not used	Z-Z1	Z1 Z Z2 → .
5	10/12	1 - 8 2 - 7 3 - 6 4 - 5	IR6 assigned to 8255 (PC3) IR6 assigned to 8255 (PC0) IR5 assigned to KBTR RS 232 TR	1 - 8 3 - 6	8 7 6 5 ↓ . ↓ . 1 2 3 4
6	1/12	X1 - X8 X2 - X7 X3 - X6 X4 - X5	Closed: 4 colour video Open: 8 colour video Closed: No memory expansion BDS Open: Memory expan- sion BDS Closed: Colour video Open: B/W video Closed: 32 KB expan- sion BDS Open: 128 KB expan- sion BDS	X1 - X8	X 8 X 7 X 6 X 5 ↓ . ↓ . ↓ X1 X 2 X 3 X 4 B/W video, no 32 KB expansion boards ----- X8 X 7 X 6 X 5 ↓ . ↓ . ↓ X1 X 2 X 3 X 4 B/W video, one two or three 32 KB expansion boards -----

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
					X 8 X 7 X 6 X 5 : : : : X 1 X 2 X 3 X 4 Colour video, one, two or three 32 KB expansion boards -----
7	9/12	D	Closed: Centronics interface	D - 1	
8	8/12	Y1 - 24 Y2 - 23 Y3 - 22 Y4 - 21 Y5 - 20 Y6 - 19 Y7 - 18 Y8 - 17 Y9 - 16 Y10 - 15 Y11 - 14 Y12 - 13	TXD (to DCE) RXD (to DTE) RXD (to DCE) TXD (to DTE) DTR (to DCE) DSR (to DTE) DSR (to DCE) DTR (to DTE) RTS (to DCE) CTS (to DTE) CTS (to DCE) RTS (to DTE)	Y1 - 24 Y3 - 22 Y5 - 20 Y7 - 18 Y9 - 16 Y11 - 14	
9	8/12	T - T1 T - T2 S - S1 S - S2 R - R1 R - R2 N - N2	CTS enabled CTS controlled by external device RTS always enabled RTS controlled by U129 (USART RS 232) DTR controlled by U129 (RS 232) DTR controlled by U110 (K1B interface) RXC generated exter- nally	T - T1 S - S2 R - R1	

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
9	8/12	P1 - N1 P - P1 P2 - N2	TXC generated exter- nally TXC internal RXC internal	P - P1 P2 - N2	
10	2/12	U - 1 U - 2	Memory Speed Timing Not used	U - 1	1 U 2 → .
11	4/12	M - M1 M - M2	128 KB RAM on mother- board (using 64K bit chip) 32 KB RAM on mother- board (using 16 K bit chip)	M - M1	M1 M M2 → .
12	2/12	W - 1 W - 2	512 KB RAM System 128-224 KB RAM System	W - 2	2 ↓ W ↓ .
13	4/12	L - L1 L - L2	M20 using single volt- age 16K bit or 64K bit RAM chips M20 using three volt- age 16K bit RAM chips	L - L1	L1 L L2 → .
14	4/12	J - J1 J - J2	For providing +12 V to three voltage 16K bit RAM chips For providing +5 V to single voltage 16K bit or 64K bit chips	J - J2	J1 J J2 . → .
15	4/12	H - H1 H - H2	For providing -5 V to three voltage 16K bit RAM chips For providing +5 V to single voltage 16K bit or 64K bit chips	H - H2	H1 H H2 . → .

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
16	4/12	U86 B	For 64 Kbit chips on motherboard	OPEN (OFF)	
17	2/12	V - 1 V - 2	128 KB - 224 KB RAM System 512 KB RAM System	V - 1	
18	6/12	E - E1 E - E2	4 colours for M20 8 colours for M20	E - E1	
19	6/12	G - G1 G - G2	Extended oscillator for testing purposes Internal 12 MHz osc for Dot clock	G - G2	

2.9.7 LEVEL D MOTHERBOARD



REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
1	12/12	F - F1 F - F2	Internal 16 MHz clock External clock	F - F1	F1 F F2 → .
2A	7/12	A - A1 A - A2	ROM 2732, 2764, MK 3700 ROM 2716	A - A1	A1 A A2 → .
2B	7/12	B - b1 B - B2	Dynamic ROM MK 3700 Static ROM/EPROM	B - B2	B1 . b2 . →
3	2/12	K - K1 K - K2	512 KB System 128 - 224 KB System	K - K2	1 K 2 . →
4	10/12	Z - Z1 Z - Z2	M20 with or without expansion board Not used	Z - Z1	Z1 Z Z2 → .
5	10/12	1 - 8 2 - 7 3 - 6 4 - 5	IR6 assigned to 8255 (PC3) IR6 assigned to 8255 (PC0) IR5 assigned to KETR IR5 assigned to RS 232 TR	1 - 8 3 - 6	8 7 6 5 ↓ . ↓ . 1 2 3 4
6	1/12	X1 - X8 X2 - X7 X3 - X6 X4 - X5	Closed: 4 colour video Open: 8 colour video Closed: No memory expansion BDS Open: Memory expansion BDS Closed: Colour video Open: B/W video Closed: 32 KB expansion BDS Open: 128 KB expansion BDS	X1 - X8	8 X 7 X 6 X 5 X . ↓ . ↓ X1 X 2 X 3 X 4 B/W video, no 32 KB expansion boards ----- X8 X 7 X 6 X 5 . . . ↓ X1 X 2 X 3 X 4 B/W video, one two or three 32 KB expansion boards -----

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
					Colour video, one, two or three 32 KB expansion boards -----
7	9/12	D	Closed: Centronics interface	D - 1	
8	8/12	Y1 - 24 Y2 - 23 Y3 - 22 Y4 - 21 Y5 - 20 Y6 - 19 Y7 - 18 Y8 - 17 Y9 - 16 Y10 - 15 Y11 - 14 Y12 - 13	TXD (to DCE) RXD (to DTE) RXD (to DCE) TXD (to DTE) DTR (to DCE) DSR (to DTE) DSR (to DCE) DTR (to DTE) RTS (to DCE) CTS (to DTE) CTS (to DCE) RTS (to DTE)	Y1 - 24 Y3 - 22 Y5 - 20 Y7 - 18 Y9 - 16 Y11 - 14	
9	8/12	T - T1 T - T2 S - S1 S - S2 R - R1 R - R2 N - N2	CTS enabled CTS controlled by external device RTS always enabled RTS controlled by U129 (USART RS 232) DTR controlled by U129 (RS 232) DTR controlled by U110 (KIB interface) RXC generated exter- nally	T - T1 S - S2 R - R1	

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
9	8/12	P1 - N1	TXC generated externally		
		P - P1	TXC internal	P - P1	
		P2 - N2	RXC internal	P2 - N2	
10	2/12	U - 1	Memory Speed Timing	U - 1	1 U ? —•
		U - 2	Not used		
11	4/12	M - M1	128 KB RAM on mother-board (using 64K bit chip)	M - M1	M1 M M2 —•
		M - M2	32 KB RAM on mother-board (using 16 K bit chip)		
12	2/12	W - 1	512 KB RAM System		2 ↓ •
		W - 2	128-224 KB RAM System	W - 2	W • •
13	4/12	L - L1	M20 using single voltage 16K bit or 64K bit RAM chips	L - L1	
		L - L2	M20 using three voltage 16K bit RAM chips		L1 L L2 —•
14	4/12	J - J1	For providing +12 V to three voltage 16K bit RAM chips		J1 J J2 • —•
		J - J2	For providing +5 V to single voltage 16K bit or 64K bit chips	J - J2	
15	4/12	H - H1	For providing -5 V to three voltage 16K bit RAM chips		H1 H H2 • —•
		H - H2	For providing +5 V to single voltage 16K bit or 64K bit chips	H - H2	

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
16	4	U86 A	Open: 32 KB memory expansion board Closed: 128 KB memory expansion board	OPEN (OFF)	
16 B	4	U85	For 64K bit RAM chips on motherboard	CLOSED (ON)	
17	2/12	V - 1 V - 2	128 KB - 224 KB RAM System 512 KB RAM System	V - 1	
18	6/12	E - E1 E - E2	4 colours for M20 8 colours for M20	E - E1	
19	6/12	G - G1 G - G2	Extended oscillator for testing purposes Internal 12 MHz osc for Dot clock	G - G2	
20	12/12	AA	Open: for producing testing Closed: normal ope- ration	AA - 1	

REFERENCE	LOGIC DIAGRAM	JUMPER	FUNCTION	NORMAL POSITION	
21	1/12	ZA - 1	Bypass power up diagnostics		1 ZA 2
		ZA - 2	Power up diagnostics run every time M20 switched on or reset	ZA - 2	• ———>

<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">RS 232 C INTERFACE</th> </tr> <tr> <td>Rx C EXTERNAL</td> <td>N - N2</td> </tr> <tr> <td>Tx C EXTERNAL</td> <td>P1 - N1</td> </tr> <tr> <td>Tx C INTERNAL</td> <td>P - P1 *</td> </tr> <tr> <td>Rx C INTERNAL</td> <td>P2 - N2 *</td> </tr> <tr> <td>DTR CONTROLLED BY U129 (USART RS 232 C INTERF.)</td> <td>R - R1 *</td> </tr> <tr> <td>DTR CONTROLLED BY U110 (USART KEYBOARD)</td> <td>R - R2</td> </tr> <tr> <td>RTS ALWAYS ENABLED</td> <td>S - S1</td> </tr> <tr> <td>RTS CONTROLLED BY U129</td> <td>S - S2 *</td> </tr> <tr> <td>CTS ALWAYS ENABLED</td> <td>T - T1 *</td> </tr> <tr> <td>CTS CONTROLLED BY EXTERNAL DEVICE</td> <td>T - T2</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">RS 232 + MODEM + PERIPHERAL CONN.</th> </tr> <tr> <td>TXD</td> <td>Y1 - 24 *</td> </tr> <tr> <td>RXD</td> <td>Y3 - 22 *</td> </tr> <tr> <td>DTR</td> <td>Y5 - 20 *</td> </tr> <tr> <td>DSR</td> <td>Y7 - 18 *</td> </tr> <tr> <td>RTS</td> <td>Y9 - 16 *</td> </tr> <tr> <td>CTS</td> <td>Y11 - 14 *</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">CENTRONIC INTERF.</th> </tr> <tr> <td>D - 1</td> <td>JUMPER ALWAYS CLOSED</td> </tr> </table>	RS 232 C INTERFACE		Rx C EXTERNAL	N - N2	Tx C EXTERNAL	P1 - N1	Tx C INTERNAL	P - P1 *	Rx C INTERNAL	P2 - N2 *	DTR CONTROLLED BY U129 (USART RS 232 C INTERF.)	R - R1 *	DTR CONTROLLED BY U110 (USART KEYBOARD)	R - R2	RTS ALWAYS ENABLED	S - S1	RTS CONTROLLED BY U129	S - S2 *	CTS ALWAYS ENABLED	T - T1 *	CTS CONTROLLED BY EXTERNAL DEVICE	T - T2	RS 232 + MODEM + PERIPHERAL CONN.		TXD	Y1 - 24 *	RXD	Y3 - 22 *	DTR	Y5 - 20 *	DSR	Y7 - 18 *	RTS	Y9 - 16 *	CTS	Y11 - 14 *	CENTRONIC INTERF.		D - 1	JUMPER ALWAYS CLOSED	MOTHER BOARD REV D4 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">AUTODIAG.</th> </tr> <tr> <td>ZA - 1</td> <td>BY PASS AUTODIAG.</td> </tr> <tr> <td>ZA - 2</td> <td>AUTODIAG.</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">AA</th> </tr> <tr> <td>PRODUCTION TESTING</td> <td>OPEN</td> </tr> <tr> <td>NORMAL OPERATION</td> <td>CLOSED</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">ROM/EPROM TYPE</th> </tr> <tr> <td>2732, 2764, MK 37000</td> <td>A - 1 *</td> </tr> <tr> <td>2716</td> <td>A - 2</td> </tr> <tr> <td>DYNAMIC ROM MK 37000</td> <td>B - 1</td> </tr> <tr> <td>STATIC ROM/EPROM</td> <td>B - 2 *</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">OSCILLATOR</th> </tr> <tr> <td>F - 1</td> <td>JUMPER ALWAYS CLOSED</td> </tr> <tr> <td>G - 2</td> <td></td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">INTERRUPT PRIORITIES</th> </tr> <tr> <td>IR6 ASSIGNED TO 8256 A (BIT 3)</td> <td>1 - 8 *</td> </tr> <tr> <td>IR6 ASSIGNED TO 8256 A (BIT 0)</td> <td>2 - 7</td> </tr> <tr> <td>IR6 ASSIGNED TO K/B TRANSM. INT.</td> <td>3 - 6 *</td> </tr> <tr> <td>IR6 ASSIGNED TO RS 232 TRANS. READY</td> <td>4 - 5</td> </tr> </table>	AUTODIAG.		ZA - 1	BY PASS AUTODIAG.	ZA - 2	AUTODIAG.	AA		PRODUCTION TESTING	OPEN	NORMAL OPERATION	CLOSED	ROM/EPROM TYPE		2732, 2764, MK 37000	A - 1 *	2716	A - 2	DYNAMIC ROM MK 37000	B - 1	STATIC ROM/EPROM	B - 2 *	OSCILLATOR		F - 1	JUMPER ALWAYS CLOSED	G - 2		INTERRUPT PRIORITIES		IR6 ASSIGNED TO 8256 A (BIT 3)	1 - 8 *	IR6 ASSIGNED TO 8256 A (BIT 0)	2 - 7	IR6 ASSIGNED TO K/B TRANSM. INT.	3 - 6 *	IR6 ASSIGNED TO RS 232 TRANS. READY	4 - 5	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">4 COLOUR DISPLAY WITH 32K MEM. EXP.</th> </tr> <tr> <td>X1 - X8</td> <td>OFF</td> </tr> <tr> <td>X2 - X7</td> <td>OFF</td> </tr> <tr> <td>X3 - X6</td> <td>ON</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">128KB ON MOT. BD/32KB ON MEM. EXP. BD</th> </tr> <tr> <td>Z - Z1, K - K2 E - E1 V - V1 W - W2, m - m1 J - J2 L - L1 U - U1 X4 - X5 H - H2 U85</td> <td>JUMPER ALWAYS CLOSED</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">B/W DISPLAY No. MEM EXP.</th> </tr> <tr> <td>X1 - X8</td> <td>OFF</td> </tr> <tr> <td>X2 - X7</td> <td>ON</td> </tr> <tr> <td>X3 - X6</td> <td>OFF</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">B/W DISPLAY WITH 32 KB MEM. EXP.</th> </tr> <tr> <td>X1 - X8</td> <td>OFF</td> </tr> <tr> <td>X2 - X7</td> <td>OFF</td> </tr> <tr> <td>X3 - X6</td> <td>OFF</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2">U96A</th> </tr> <tr> <td colspan="2">MEMORY EXP. 32K OR 128K</td> </tr> <tr> <td>32K MEM EXP.</td> <td>ALL JUMPERS OPEN</td> </tr> <tr> <td>128K MEM. EXP.</td> <td>ALL JUMPERS CLOS.</td> </tr> </table> + PERIPHERAL CABLE CODE: 336085 T MODEM CABLE CODE : 334922 L * NORMALLY CLOSED BY FACTORY	4 COLOUR DISPLAY WITH 32K MEM. EXP.		X1 - X8	OFF	X2 - X7	OFF	X3 - X6	ON	128KB ON MOT. BD/32KB ON MEM. EXP. BD		Z - Z1, K - K2 E - E1 V - V1 W - W2, m - m1 J - J2 L - L1 U - U1 X4 - X5 H - H2 U85	JUMPER ALWAYS CLOSED	B/W DISPLAY No. MEM EXP.		X1 - X8	OFF	X2 - X7	ON	X3 - X6	OFF	B/W DISPLAY WITH 32 KB MEM. EXP.		X1 - X8	OFF	X2 - X7	OFF	X3 - X6	OFF	U96A		MEMORY EXP. 32K OR 128K		32K MEM EXP.	ALL JUMPERS OPEN	128K MEM. EXP.	ALL JUMPERS CLOS.
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DSR	Y7 - 18 *																																																																																																																			
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128K MEM. EXP.	ALL JUMPERS CLOS.																																																																																																																			

2.9.8 LEVEL D5 MOTHERBOARD

The level D5 motherboard is identical to the D4 motherboard with the exception of the following jumpers which are now soldered:

!-----!	
! FIXED JUMPERS !	! FUNCTION !
!-----!	
! Y1 - Y24	! These jumpers
! Y3 - Y22	! used to discriminate
! Y5 - Y20	! between modem or
! Y7 - Y18	! peripheral connection
! Y9 - Y16	! for the RS 232C
! Y11- Y14	! interface
!-----!	
! A - A2	! Use of ROM 2732
! B - B2	!
!-----!	
! H - H2	! Use of 64K bit
! J - J2	! RAM chips
! L - L1	!
!-----!	
! U -U1	! 200nsec memory timing
! U85 ON	! Type of RAM used
!-----!	

2.9.9 MOTHERBOARDS WITH BOOTSTRAP ROM REV. 2.0

With the Bootstrap ROM REV 2.0 three mini-floppy disk drive configurations are possible. These are:

- 160 Kbyte Mini-Floppy Disk Drive(s)
- 320 Kbyte mini-Floppy Disk Drive(s)
- 640 Kbyte Mini-Floppy Disk Drive(s)

The mini-floppy disk drive jumper configurations are as follows:

X4 to X5	*ZA to	FUNCTION
ON	ZA1	Skip diagnostics and query user for mini-floppy disk type
ON	ZA2	160KB Mini-Floppy Drive(s)
ON	ZA1	320KB Mini-Floppy Drive(s)
ON	ZA2	640KB Mini-Floppy Drive(s)

* For 'CP' level motherboards (i.e. motherboards where no ZA jumper is present) jumper B is used instead. ZA - ZA1 is hence equivalent to B - 1.

D6 = X4 to X5 = OFF

2.9.10 SUMMARY OF JUMPER CHARTS FOR VARIOUS MEMORY CONFIGURATIONS

CONFIGURATION	Z1-Z22	K1-K-K2	E1-E-E2	V1-V-V2	W1-W-W2	M1-M-M2	X1 - X8	X2 - X7	X3 - X6	U62/3/4/5	U86 A
M 20 WITH OUT ANY EXPANSION BOARDS	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	ON	OFF	ICs PRESENT	OFF
M 20 WITH AT LEAST ONE B/W 32KB EXPANSION BOARD	Z - Z1	K - K 2	E - E1	V - V1	W - W2	M - M1	OFF	OFF	OFF	ICs PRESENT	OFF
M 20 WITH AT LEAST ONE B/W 128KB EXPANSION BOARD	Z - Z1	K - K1	E - E1	V - V2	W - W1	M - M2	ON	OFF	OFF	ICs NOT PRESENT	ON
M 20 WITH ONE 32KB COLOUR BOARD (4 COLOURS)	Z - Z1	K - K2	E - E1	V - V1	W - W2	M - M1	OFF	OFF	ON	ICs PRESENT	OFF
M 20 WITH ONE 128KB COLOUR BOARD (4 COLOURS)	Z - Z1	K - K1	E - E1	V - V2	W - W1	M - M2	OFF	ON	ON	ICs NOT PRESENT	ON
M 20 WITH TWO 32KB COLOUR BOARDS (8 COLOURS)	Z - Z1	K - K2	E - E2	V - V1	W - W2	M - M1	ON	OFF	ON	ICs PRESENT	OFF
M 20 WITH TWO 128KB COLOUR BOARDS (8 COLOURS)	Z - Z1	K - K1	E - E2	V - V2	W - W1	M - M2	ON	ON	ON	ICs NOT PRESENT	ON

2.9.11 HARD DISK CONTROLLER JUMPERS

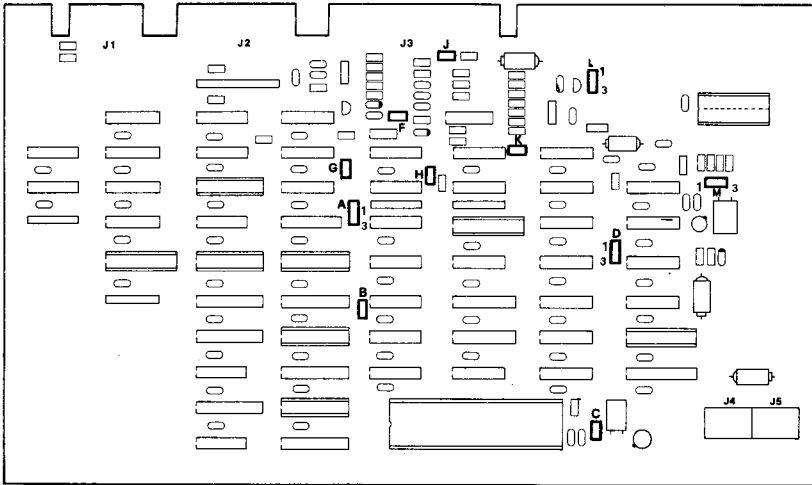


Fig. 2-24 Hard Disk Controller Board

JUMPERS CLOSED

L1-2
M1-2
D2-3
C
B
A1-2

JUMPERS OPEN

G
H
K
J
F

N.B. The above jumpers should not be touched except when performing the Hard Disk Controller Adjustments (see chapter 3).

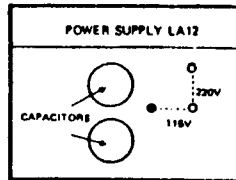
83.10

3874272 S 23/A

BIT

KEYBOARD	
COUNTRY	JUMPERS
	29 28 27 26
ITALY	X X X X
W. GERMANY	X X X
FRANCE	X X X
U.K.	X X
USA ASCII BASIC	X X X
SPAIN	X X
PORTUGAL	X X
SWEDEN/FINLAND	X X
DENMARK	X X X
KATAKANA	X X
NORWAY	X
SWITZERLAND - F	X
SWITZERLAND - D	X

NOTE: X = CLOSED



MEMORY EXPANSION 32KB	
J1	B - C
J2	A - B
J3	A - B
J4	B - C
JUMPER ALWAYS CLOSED	

13A/90

MOTHER BOARD BILAYER NABC G-SERIES

HS 232 C INTERFACE	
R ₁ C EXTERNAL	N - N2
T ₁ C EXTERNAL	P1 - N1
T ₁ C INTERNAL	P - P1
R ₁ C INTERNAL	P2 - N2
DTR CONTROLLED BY U129 (USART)	R - R1
DSR CONTROLLED BY U110 (USART)	R - R2
RTS ALWAYS ENABLED	B - B1
RTS CONTROLLED BY U129	S - S2
CTS ALWAYS ENABLED	T - T1
CTS CONTROLLED BY EXTERNAL DEVICE	T - T2

CENTRONIC INTERF.	
D - 1	JUMPER ALWAYS CLOSED

- 4 PERIPHERAL CABLE CODE 33606 T
MODERN CABLE CODE 33602 L
- 4 NORMALLY CLOSED BY FACTORY

SYSTEM CONFIGURATION		
ZA - 1	X4 - X5	
ON	ON	BY PASS AUTODIAG
OFF	ON	FLOPPY 160KB
ON	OFF	FLOPPY 320KB
OFF	OFF	FLOPPY 640KB

COLOR DISPLAY	E1 - E2
4 COLOR	E - E1
8 COLOR	E - E2

OSCILLATOR	
G - 1	CR EXTERNAL
G - 2	CR INTERNAL

INTERRUPT PRIORITIES	PATCH
IR6 ASSIGNED TO 8256 A (BIT 3)	1 - 8
IR6 ASSIGNED TO 8256 A (BIT 0)	2 - 7
IR5 ASSIGNED TO K/B TRANSF. INT.	3 - 8
IR6 ASSIGNED TO RS 232 TRANS. READY	4 - 8

B/W DISPLAY WITH	
32 KB MEM. EXP.	128 KB MEM. EXP.
X1 - X8	OFF ON
X2 - X7	OFF OFF
X1 - X6	OFF OFF

128KB ON MOT. BD/32KB ON MEM. EXP. BD	
E - E1	V - V1
W - W2	m - m1
JJ 3 - 2	JUMPER ALWAYS CLOSED

128KB ON MOT. BD/128KB ON MEM. EXP. BD	
E - E1	K - K1
W - W1	V - V2
JJ 1 - 2	JUMPER ALWAYS CLOSED

B/W DISPLAY No. MEM. EXP.	
X1 - X8	OFF
X2 - X7	ON
X3 - X6	OFF

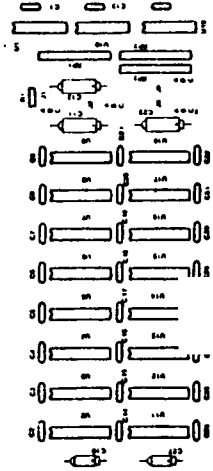
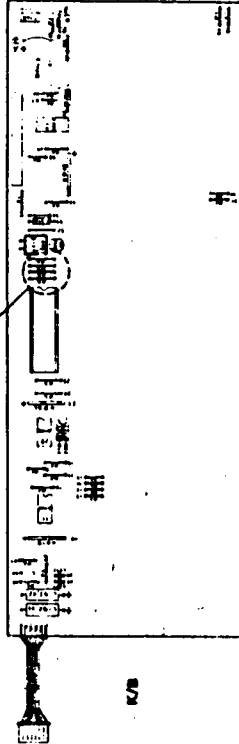
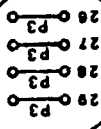
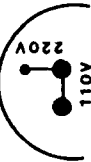
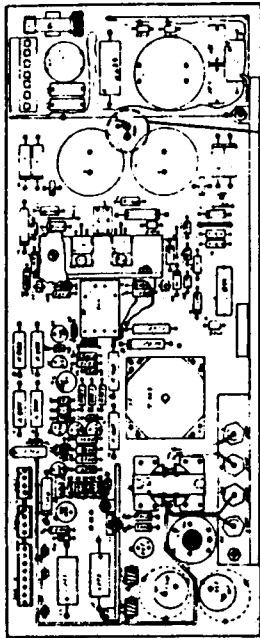
F - 1	JUMPER ALWAYS CLOSED
D - U	
I - F	

C-C Open

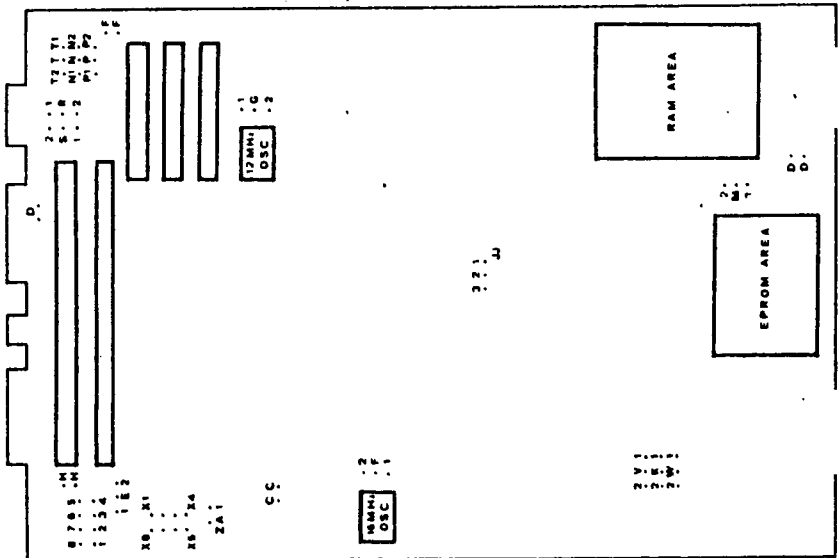
COLOR DISPLAY WITH			
32KB MEM. EXP.		128KB MEM. EXP.	
4 COLOR	8 COLOR	4 COLOR	8 COLOR
X1 - X8	OFF OFF	ON OFF	ON
X2 - X7	OFF OFF	ON ON	ON
X3 - X6	ON ON	ON ON	ON

olivetti Prodotto L1M20 Data 11/2/82	Designazione M20 - JUMPER CONFIGURATION	Mod. _____ Data _____	Mod. _____ Data _____	Visto _____ Visto _____
	CARTELLINO DI SPECIALIZZAZIONE Specialization Card	Mod. _____ Data _____	Mod. _____ Data _____	Visto _____ Visto _____
	Codice 335286 V	Mod. _____ Data _____	Mod. _____ Data _____	Visto _____ Visto _____
	Mod. _____ Data _____	Mod. _____ Data _____	Mod. _____ Data _____	Visto _____ Visto _____

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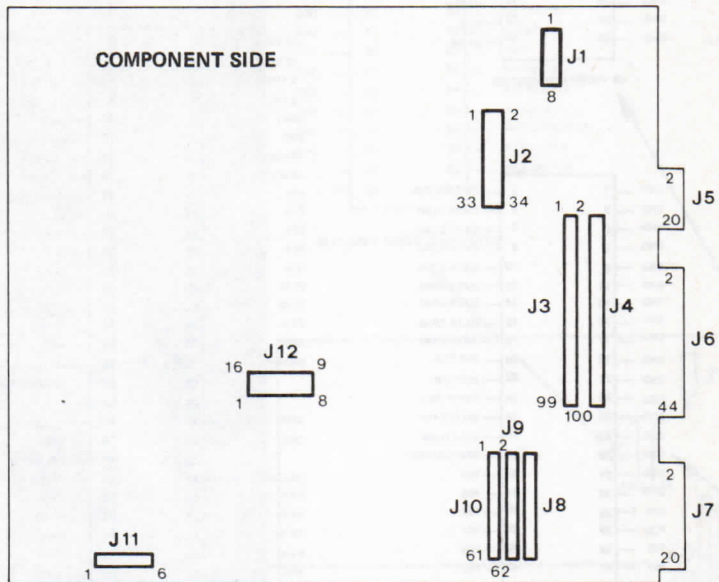


MOTHER BOARD BILAYER

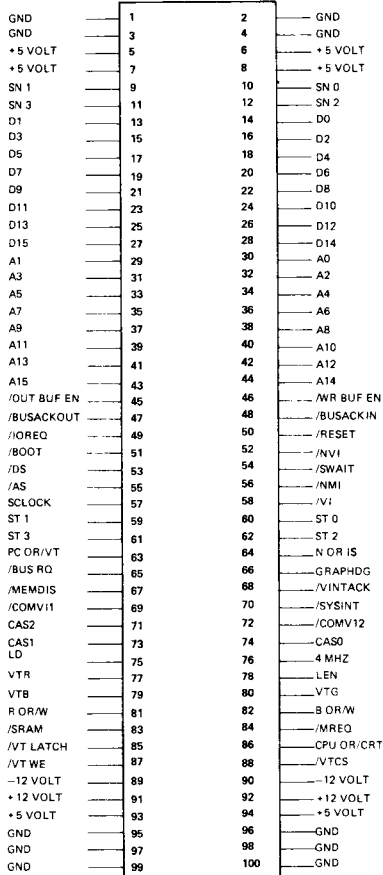


2.10 CONNECTOR DESCRIPTIONS

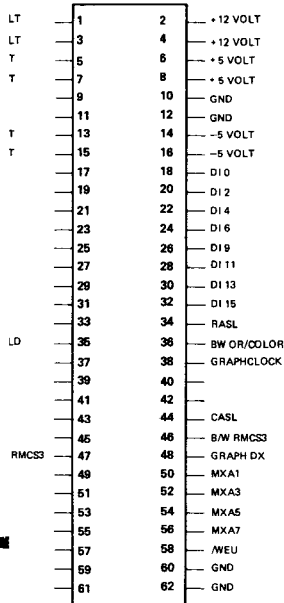
This section shows all the connectors used on the M20 motherboard.



- J1 POWER CONNECTOR
- J2 FLOPPY DISK DRIVE CONNECTOR
- J3 } BUS CONNECTOR (IEEE, VIDEOTEX, TWIN RS 232 C, APB 1086)
- J4 }
- J5 VIDEO CONNECTOR
- J6 PARALLEL INTERFACE CONNECTOR
- J7 SERIAL INTERFACE CONNECTOR (RS 232 C)
- J8 MEMORY EXPANSION BOARD CONNECTOR
- J9 MEMORY EXPANSION BOARD CONNECTOR
- J10 MEMORY EXPANSION BOARD CONNECTOR
- J11 KEYBOARD CONNECTOR
- J12 VIDEOTEX CONNECTOR



J3 AND J4 BUS CONNECTOR



J5, J6 MEMORY EXPANSION BOARD CONNECTOR

KE¹
KE²
+5
/RE
GND
+12

2.11 INSTALLATION OF EXTERNAL HARD DISK UNIT (KIT HDS 1053).

Materials Required:

External HDU Module

Hard Disk Controller attached to a Metal Base

Transition Board IF131

Signal Ribbon Cables

Power Cables

The following steps should be followed when installing an External Hard Disk Unit:

- 1) Disconnect the mains cable and any peripherals connected to the M20.
- 2) Remove the M20 cover by first loosening the two screws at the rear of the Basic Module and lifting the rear of the cover.
- 3) Remove keyboard and any optional boards present in the M20.

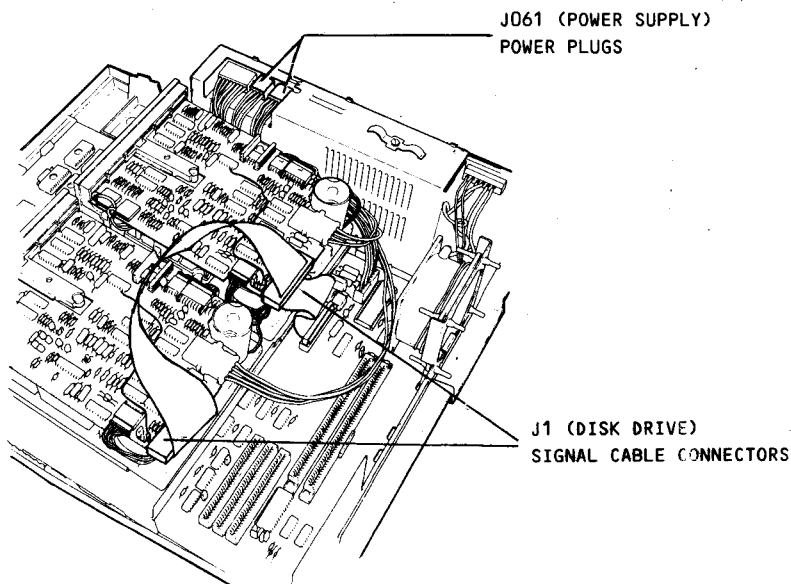


Fig. 2-25 Removal of Cable Connectors.

- 4) Remove the two signal cable connectors J1 which reside on the driver boards of drive 0 and drive 1.
- 5) Remove the power plugs for both disk drives from the M20 power supply

connector J061.

6) Remove the whole metal base of the floppy disk drives assembly by first sliding the base slightly forward and then lifting it from the basic module.

7) Check if the motherboard is at level D9. If not upgrade the motherboard to level D9 as described in BIT Code 3874277 X No. 15.

8) Remove the two minifloppy drives from the metal base by unscrewing the two screws at the front.

Fix the two floppy disks on to the new metal base, present in the kit provided, by means of the two screws removed previously. Drive 0 must be put on the right and drive 1 on the left.

9) Check that the jumper settings on the Hard Disk Controller are as shown in page 2-64.

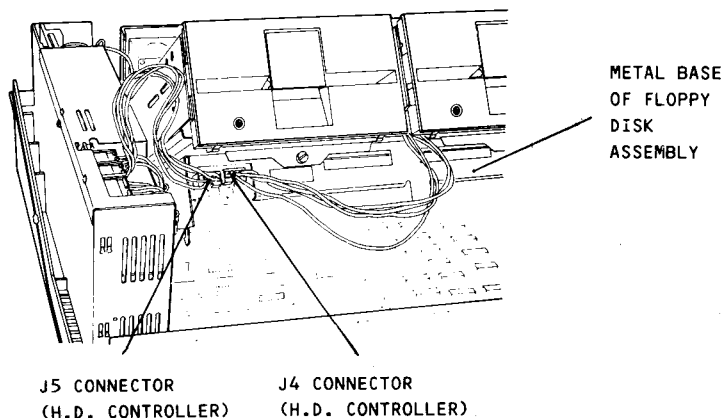


Fig. 2-26 Connection of Power Cables.

10) Place back the floppy disk assembly and connect the power cable for drive 1 (left drive). The power supply cable present in the kit must be connected from the power supply connector J061 to plug J5 on the controller. The DC power cable coming from J2 on drive 0 must go to connector J4 on the Hard Disk Controller.

11) Connect the signal cables coming from connector J2 on the motherboard to the disk drives into connector J1 of drive 0 and drive 1. Ensure that the cable connectors are orientated so that the cables exit from the bottom.

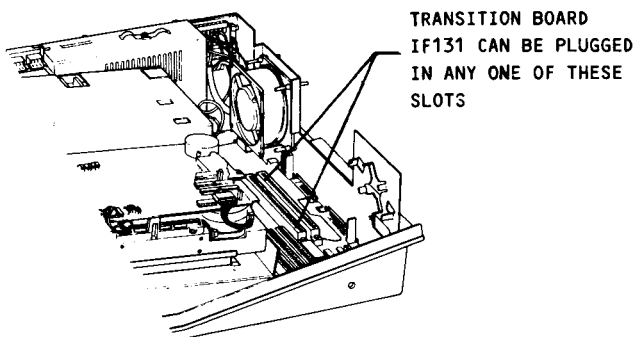


Fig. 2-27 Positioning of Transition Board.

12) Place Transition board IF131 in slots J3 or J4 on the motherboard with the components side facing the drives. Also connect the signal cable from Transition Board to J3 on the controller ensuring that the cables exit from the top.

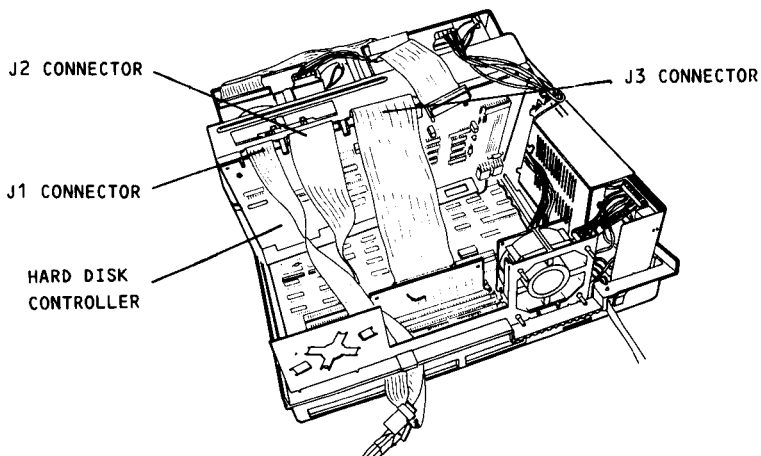


Fig. 2-28 Connecting the HDU Module to the M20

13) Pass the two cables coming from the HDU module through the slot at the back of the M20 basic module and connect them to J1 and J2 of the controller board. Ensure that the cable connectors are orientated so that the cables exit from the top.

If any memory expansion boards are present the cables must pass on the right side of the boards.

14) Replace any optional boards removed previously.

Replace the front cover of the disk drives, keyboard and the M20 cover, tightening the two screws at the back.

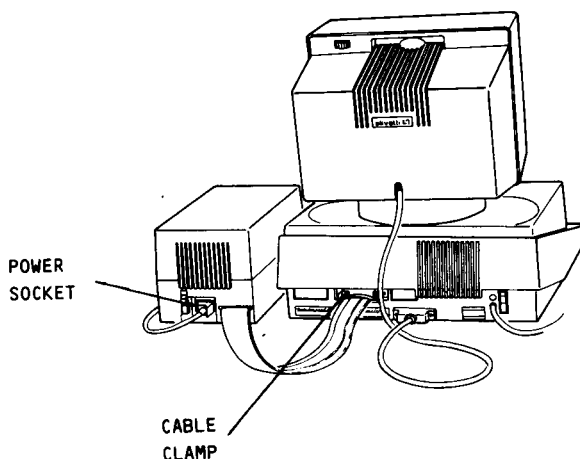


Fig. 2-29 Attaching Cable Clamp.

14) Fix the clamp attached to the cables connecting the HDU module to the M20 basic module by means of two hex screws.

15) Insert the AC mains cable, present in the kit, in the socket situated at the back of the HDU module. Check that the voltage indicated on the sticker at the rear of the HDU module is the same as at the power outlet to be used. Check that the power switch on the HDU module is off, insert the mains cable in the power outlet and switch on the power switch.

2.12 TV ADAPTER

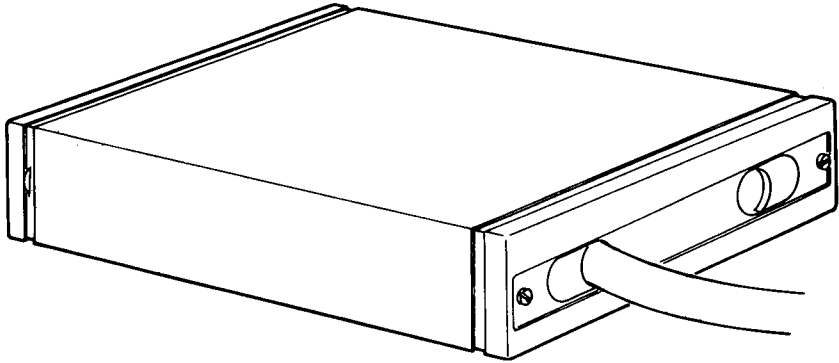


Fig. 2-30 TV Adapter

2.12.1 Installation Procedures

The following steps should be followed when installing a TV Adapter:

1. Set the jumper G present on the motherboard to receive the external 12 MHz clock coming from the TV Adapter, setting it to G1.
2. Also set the 5 jumpers present on the TV Adapter (for the clock selection and for the PAL or NSTC selection) as shown in the table of page 2-73
3. Connect the M20 to the TV Adapter by means of a signal cable which goes directly to the adapter.
4. Disconnect the 75 ohm coaxial antenna signal cable from the wall outlet and connect it to the TV Adapter.

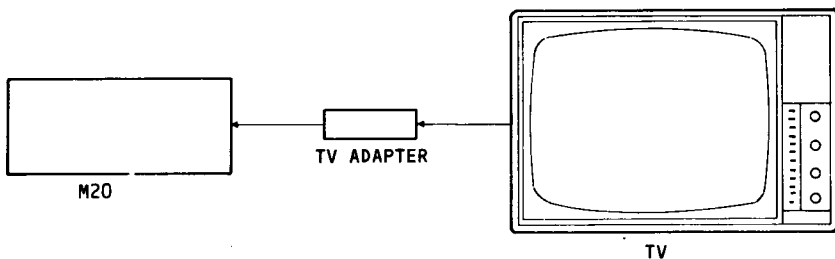


Fig. 2-31 Connection of TV Adapter

2.12.2 JUMPERS

jumpers		selections
A	2-1	PAL
A	2-3	NTSC
B	2-1	Channel 4 NTSC
B	2-3	Channel 3 NTSC
C	1-2	Clock internal
C	2-3	Clock external
D	1-2	PAL
D	2-3	NTSC
E	1-2	NTSC
E	2-3	PAL

These jumpers will be set in production for the TV Adapter to work with the PAL system. They will only be set for NTSC on specific requests.

2.12.3 ADJUSTMENTS

All adjustments are done directly in production and are NOT to be changed in the field.

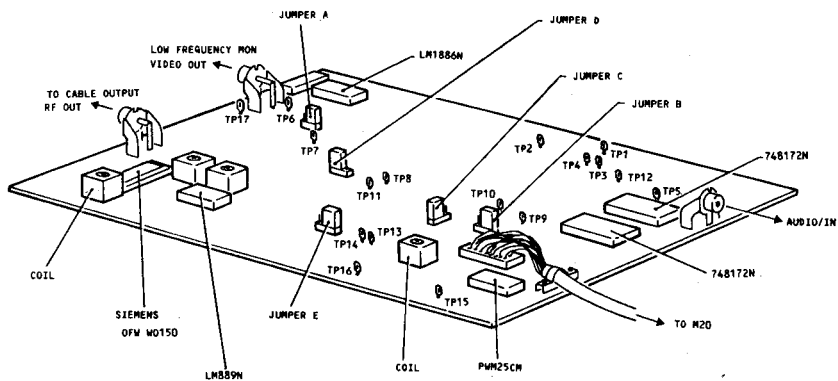


Fig. 2-32 TV Adapter board

3

MAINTENANCE

3. MAINTENANCE

3.1 INTRODUCTION

The solid state circuitry of the M20 and the minimum number of moving parts render the system virtually free from maintenance. Preventive maintenance is therefore limited to cleaning, troubleshooting, and signal verification. One should brush accumulated dust from the active areas of the system. Care should be exercised that foreign objects such as staples, pins do not fall into the keyboard.

This chapter deals with all the adjustments performed on the power supply, motherboard and hard disk controller. For signal adjustments on the CRT Displays refer to the Video General Service Manual. A list of references is given in the preface of this manual. For signal adjustments on the Mini-Floppy Disk drives refer to the "Mini-Floppy General Service Manual (code 3961640 W)" and for signal adjustments on the Hard Disk Unit refer to " 5 1/4 Hard Disk Unit Service Manual (code 3964410 V)". The second part of this chapter deals with the disassembly and assembly of the various modules.

3.2 SIGNAL ADJUSTMENTS

The signal adjustments to be performed are on the motherboard, power supply module and hard disk controller.

3.2.1 MOTHERBOARD

The only adjustment to be performed on the motherboard is the VCO (Voltage Controlled Oscillator) on the mini-floppy disk interface. The mini-floppy disk interface circuitry is found on the left side of the motherboard towards the rear. The VCO is required to separate data bits from the clock bits coming from the mini-floppy disk drive. If the VCO is not working properly, data cannot be received accurately from the mini-floppy disk drive.

This VCO adjustment should only be performed when one of the components in the mini-floppy disk interface logic is changed. In most cases it will not be necessary to perform this adjustment, but it is advisable to verify these signals when a component in the mini-floppy disk interface has been substituted. The two signals to be verified and eventually adjusted in the VCO are:

- 1) Reference voltage of 1.4 Volts

2) Oscillator frequency of 2 MHz

3.2.1.1 VCO Reference Voltage

The VCO reference voltage should always be 1.4 Volts. Set the oscilloscope for channel 1, DC, .5 msec/div, and .5 volt/div. Place the probe on TP1 (after having ensured that the ground lead of the probe is connected to a suitable ground point) and check that the signal on the oscilloscope is 1.4 Volts.

Potentiometer R5 controls this voltage. Should the voltage not be equal to 1.4 Volts, adjust R5 until the voltage is 1.4 V.

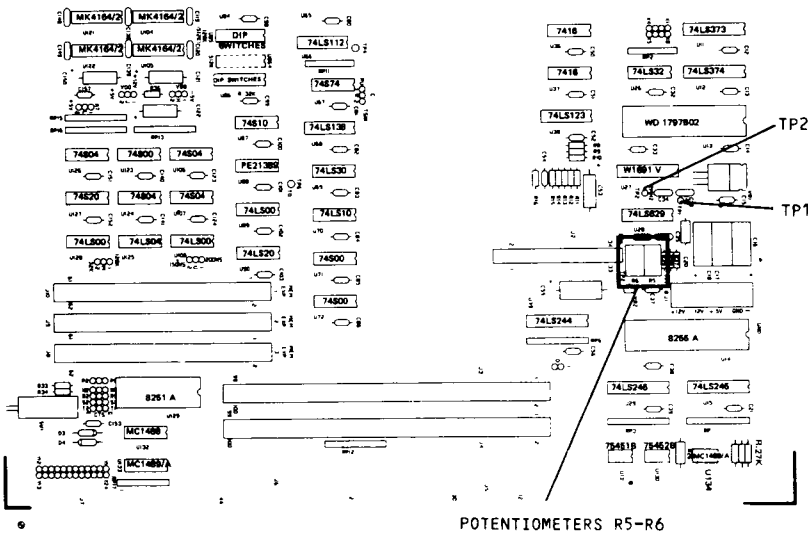


Fig. 3-1 Mini-Floppy Disk Interface section of motherboard

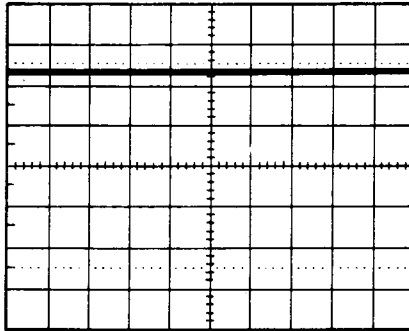


Fig. 3-2 1.4 Volts Signal Level (.5msec/div; .5 volt/div)

3.2.1.2 VC0 Frequency

The voltage controlled oscillator is a nominal 2.00 MHz master clock input to the Floppy support Logic Chip 1691. An oscilloscope is needed to verify this frequency. The test point used to measure this frequency is TP2 on the motherboard and the potentiometer R6 controls this frequency.

Set up oscilloscope for channel 1, sync internal, trigger normal, AC, TP2 and adjust the variable resistor R6 until the signal viewed on channel 1 is .5 microseconds leading edge to next leading edge i.e. 5 divisions.

Frequency = $1/\text{Period} = 1/.5\mu\text{s} = 2 \text{ MHz}$.

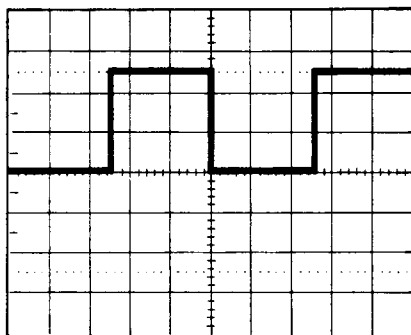


Fig. 3-3 2 MHz VCO Frequency (1usec/div; .5 volts/div)

3.2.2 POWER SUPPLY

The power supply provides +5Vdc, -12Vdc, and +12Vdc voltages. Two test points are provided on the power supply: one for the +5Vdc and the other for the +12Vdc. The only adjustment to be performed is on the +5V circuitry which in turn affects the other voltages. The adjustment is performed by means of the potentiometer found on top of the power supply cover near the DC output connectors J061.

The negative lead of the voltmeter is connected to a suitable ground point. The positive lead is connected to test point 2. The voltmeter reading should be +5 Volts. If the reading is not +5 Vdc, the potentiometer is rotated until the reading is exactly + 5Vdc. After having performed this adjustment TP1 is also controlled to verify the +12Vdc output.

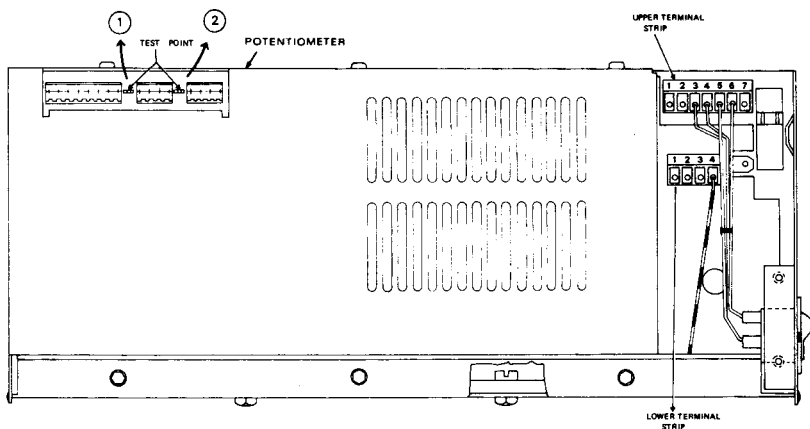


Fig. 3-4 Power Supply

3.2.3 HARD DISK CONTROLLER ADJUSTMENTS

The Hard Disk controller requires no scheduled preventive maintenance. The adjustments required re:

- DRUN (Data Run) Adjustments
- Error Amplifier Adjustments (static)
- VCO (Voltage Controlled Oscillator) Adjustments

Instruments needed are:

- a) Oscilloscope (single channel sufficient)
- b) Digital Voltmeter
- c) Frequency Counter

Also needed for the DRUN adjustment is the M20 system with one mini-floppy disk drive.

NOTE: In the following adjustments the numbers indicated in the figures refer to the steps to be performed.

3.2.3.1 DRUN Adjustments

To facilitate the process of acquiring phase lock on data being read from a disk, a hardware detector is utilized to indicate when the read/write head of the drive is over a recorded field of all ones or all zeros. The detector depends on the timing of a one-shot (8L) which is adjusted by the DRUN pot (R33). R33 must be adjusted according to the following procedures:

1 - Install jumper between M pin 2 and 3

2 - Connect the scope probe at TP 17 and set the oscilloscope to 2 Volts/division and 500usec/division.

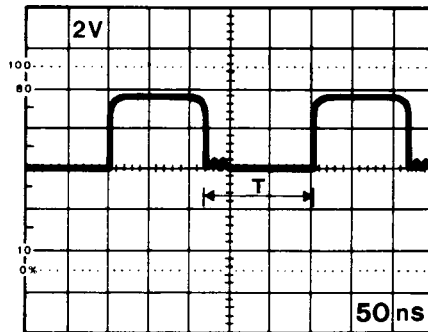


Fig. 3-6 One-shot period T smaller than 250ns

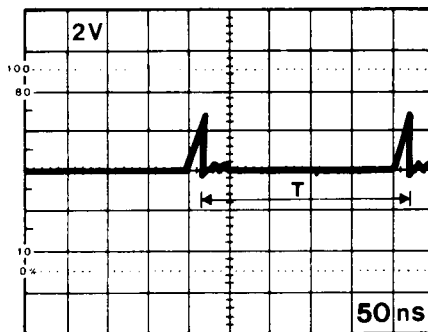


Fig. 3-7 One shot period is 250 ns

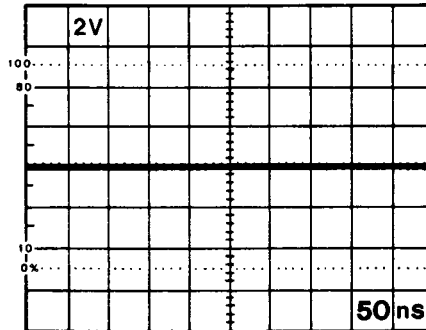


Fig. 3-8 Correct Adjustment

- 5 - Remove jumper between M pin 2 and 3
- 6 - Install jumper between M pin 1 and 2

3.2.3.2 Error Amplifier Adjustments

The phase detection technique used to correct the frequency and phase of the VCO employs a balanced sample and hold error amplifier. To ensure reliable operation of the data separator, the error amplifier must be properly balanced. The balance adjustment must be made using the following procedures:

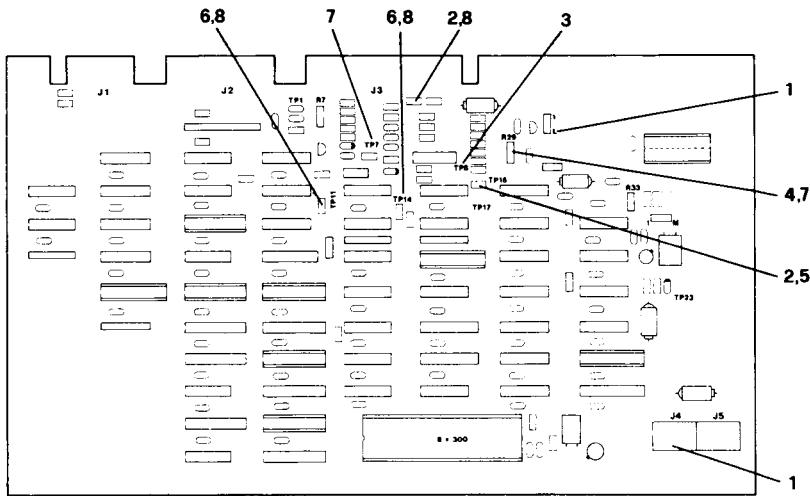


Fig. 3-9 Hard Disk Controller Board

1 - Apply power to the board. This can be achieved by connecting J4 and connecting also the signal cable that comes from the transition board to the Hard Disk Controller J3.

2 - Install jumper K and J

3 - Connect the positive lead of the voltmeter to TP8 and the negative lead to a suitable ground point (for example ground side of R27)

4 - Adjust R29 so that TP8 is within 0 + or - 20mVolts

5 - Remove jumper K

6 - Install jumper H and jumper G

7 - Connect the positive lead of the voltmeter to TP7 and adjust R29 so that the voltmeter reading is within 0 + or - 20mVolts.

8 - Remove jumper H, G and J

3.2.3.3 VCO Adjustments

Data separation circuitry on the Hard Disk Controller uses a voltage controlled oscillator (VCO) which phaselocks onto incoming data and provides

clock suitable for separating data and clock bits on an MFM encoded data stream. The VC0 must be adjusted using the following procedure:

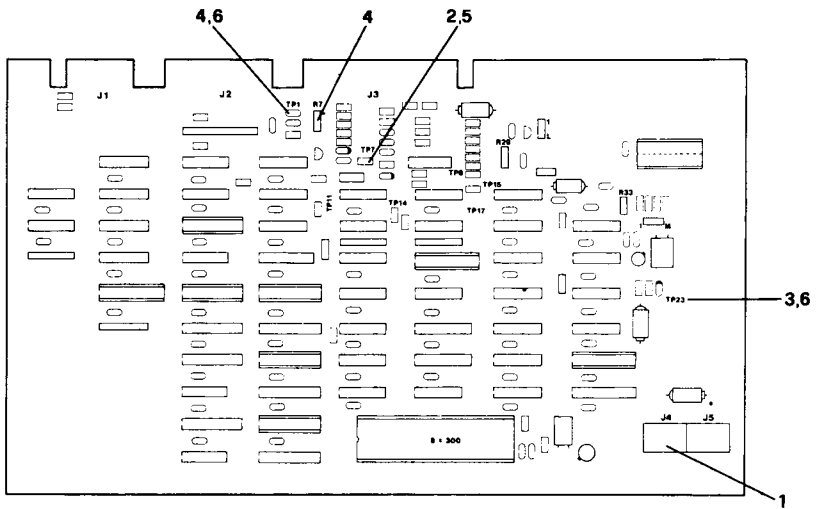


Fig. 3-10 Hard Disk Controller Board

- 1 - Apply power to the Hard Disk Controller. This can be achieved by connecting J4 and connecting the signal cable that comes from the transition board to the Hard Disk Controller connector J3.
- 2 - Install jumper F
- 3 - Connect the frequency counter at TP23. The reading should be 10MHz + or - 2kHz.
- 4 - Connect the frequency counter at TP1. Adjust R7 until the frequency measured at TP1 matches the frequency previously measured at TP23.
- 5 - Remove jumper F
- 6 - Verify once again that the frequency at TP1 and TP23 matches.

3.2.4 ADJUSTMENT ON D10 LEVEL MOTHERBOARD

Level D10 motherboards require an additional adjustment to be performed if the M20 system is equipped with a 640KB mini-floppy. Previous level motherboards do not support 640KB Disk Drives. The adjustment to be carried out concerns the precompensation frequency which is output from pin 7 of the four phase clock generator WD 2143 (U136).

To perform this adjustment run the System Test Mini-Floppy Disk Functional Test (test 6) in write mode. Place the oscilloscope probe on U136 pin 7 and the following signal must be observed. If not, adjust R51.

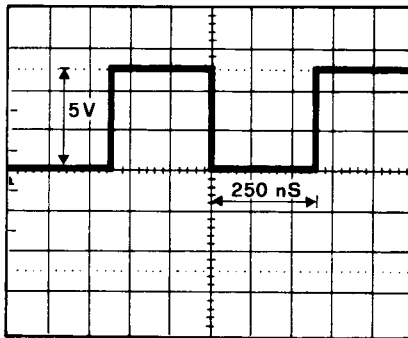


Fig. 3-11 Precompensation Frequency Adjustment

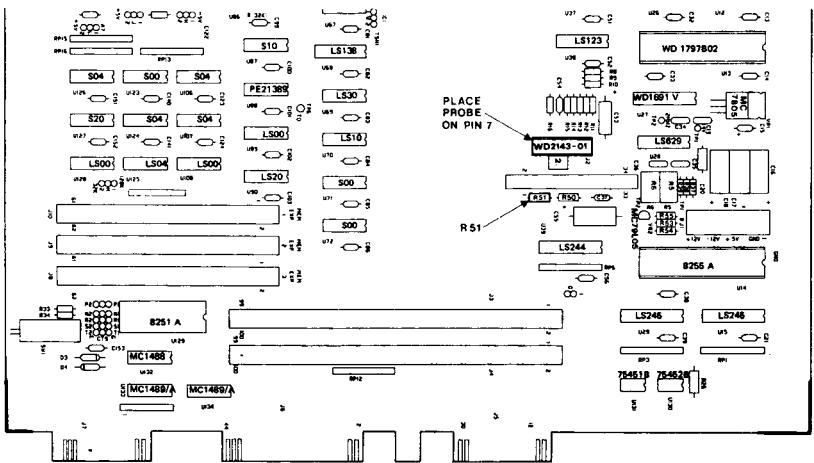


Fig. 3-12 Mini-Floppy Interface on Motherboard

3.3 DISASSEMBLY AND ASSEMBLY OF MAIN MODULES

BEFORE PROCEEDING WITH ANY DISASSEMBLY PROCEDURES MAKE SURE THAT YOUR SYSTEM IS SWITCHED OFF AND THE AC CABLE IS REMOVED FROM THE SUPPLY.

3.3.1 REPLACEMENT OF BASIC MODULE COVER

The Basic Module is protected by a cover. The cover is maintained in place at the rear by two screws.

Tools required: Screwdriver

- 1) Unplug the CRT Display and any printer connected to the system from the Basic module.
- 2) Loosen the two screws at the rear of the Basic Module cover.

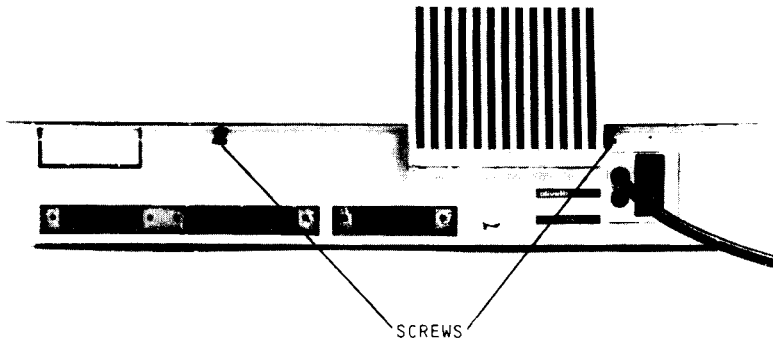


Fig. 3-13 Loosening of the two screws

- 3) Lift the rear of the cover.
- 4) Remove the whole cover.

In order to reinstall the Basic Module cover perform the same operations

in reverse.

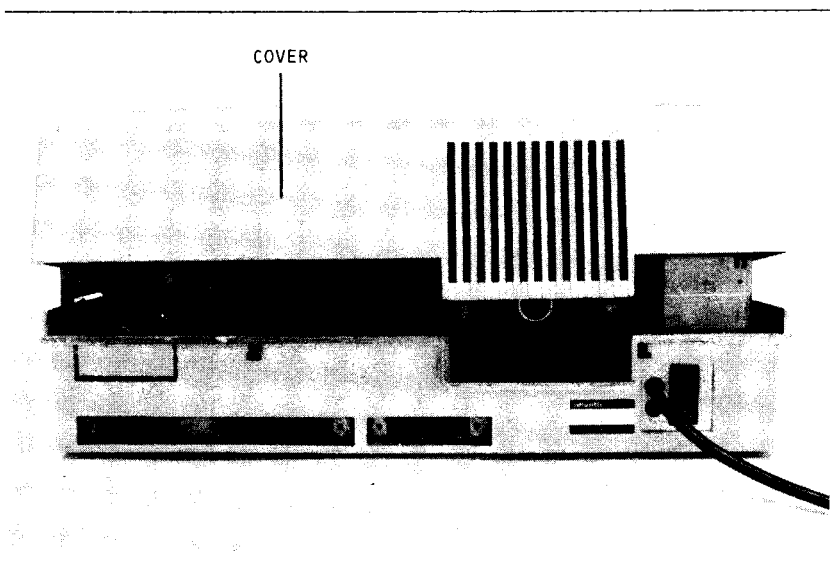


Fig. 3-14 Removal of cover

3.3.2 REPLACEMENT OF KEYBOARD

The keyboard is protected by the Basic Module cover and connected to the motherboard by means of a cable which fits into connector J11 on the motherboard. On the keyboard side the cable is already fitted.

Tools Required: Screwdriver

- 1) Unplug the CRT Display and any printer connected to the system from the Basic Module.
- 2) Remove the Basic Module cover.
- 3) Unplug the keyboard cable from connector J11 on the motherboard.
- 4) Remove the keyboard from the two locating stubs which hold it in place.

In order to reinstall the keyboard, perform the same operation in reverse.

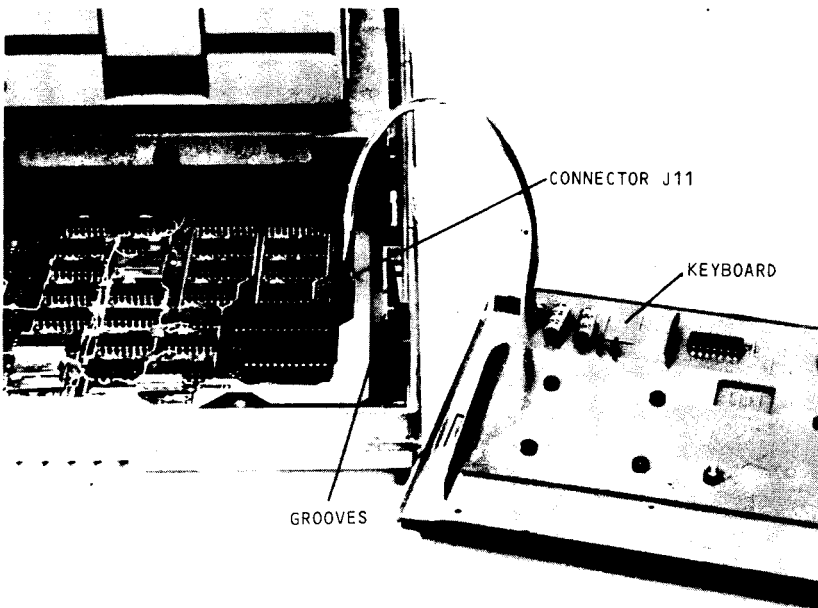


Fig. 3-15 Removal of keyboard

3.3.3 REPLACEMENT OF MINI-FLOPPY DISK DRIVE(S)

The M20 can either have one or two mini-floppy disk drives. The procedure for removing one disk drive is as follows:

Tools Required: Screwdriver

- 1) Unplug the CRT Display and any printer that may be connected to the Basic Module
- 2) Remove the Basic Module cover, keyboard, and front disk cover
- 3) Remove the ribbon connector from J2 on the motherboard and from J1 on the disk drive printed circuit board.
- 4) Remove the power connector from disk drive connector J2. J2 is the disk drive DC power connector located near the spindle drive motor and mounted on the component side of the disk drive printed circuit board.
- 5) Remove the whole metal base of the mini-floppy disk drive by first sliding the base slightly forward and then lifting the base from the Basic Module
- 6) Remove the mini-floppy disk drive from the base by loosening the screw on the front of the metal base

Reinstall the disk drive by performing the same operations in reverse

The procedure for removing the two disk drives is as follows:

- 1) Unplug the CRT Display and any printer that may be connected to the Basic Module
- 2) Remove the Basic Module cover, keyboard and front disk cover.
- 3) Remove the ribbon connector from J2 on the motherboard.
- 4) Remove the power connector from disk drive 0. (connector J2 on the disk drive printed circuit board)
- 5) Remove the power connector from disk drive 1. (connector J2 on the disk drive printed circuit board)
- 6) Remove the whole metal base of the mini-floppy disk drives by first sliding the base gently forward and then lifting the base from the Basic Module.
- 7) Remove the mini-floppy disk drives from the metal base by loosening the two screws on the front of the metal base.

Reinstall the disk drives by performing the same operations in reverse.

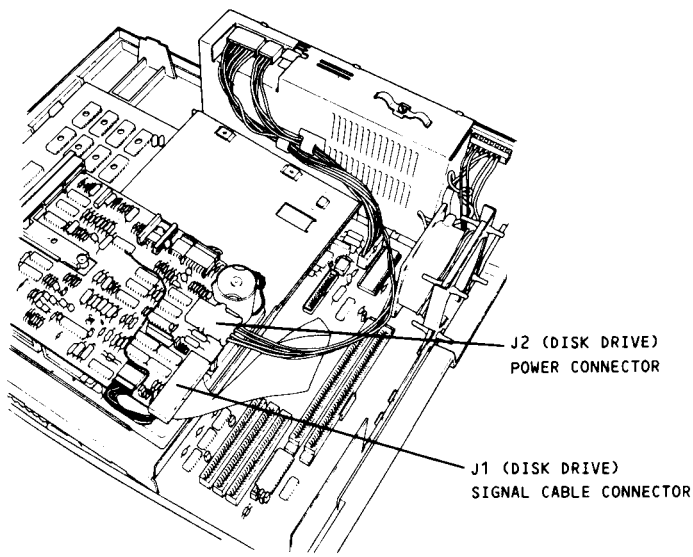


Fig. 3-16 Removal of mini-floppy disk drive

3.3.4 REPLACEMENT OF POWER SUPPLY UNIT

The power supply is mounted on the left side of the Basic Module. It is connected to the motherboard and to the mini-floppy disk drive(s).

Tools Required: Screwdriver

- 1) Unplug the CRT Display and any printer that may be connected to the system from the Basic Module.
- 2) Remove the Basic Module cover.
- 3) Remove the front disk cover and keyboard.
- 4) Unplug the cable that connects the power supply to the motherboard from connector J064 on the power supply.
- 5) Unplug the cable(s) that connect(s) the power supply to the mini-floppy disk drive(s) from connector(s) J061 on the power supply.
- 6) Remove the wires which connect the power supply to the fan from the upper and lower terminal strips:
Earth wire (Green/Yellow) is disconnected from the lower terminal strip pin 3
One supply wire (Black) is connected from the upper terminal strip pin 1
The other supply wire (Black) is connected from the upper terminal strip pin 2
- 7) Remove the power supply unit from the Basic Module by sliding it forward until it is released from the locating studs on the base of the machine
- 8) Extract the power supply unit.

9) Remove the mains power cable (see section 3.3.7 steps 3,5,6)

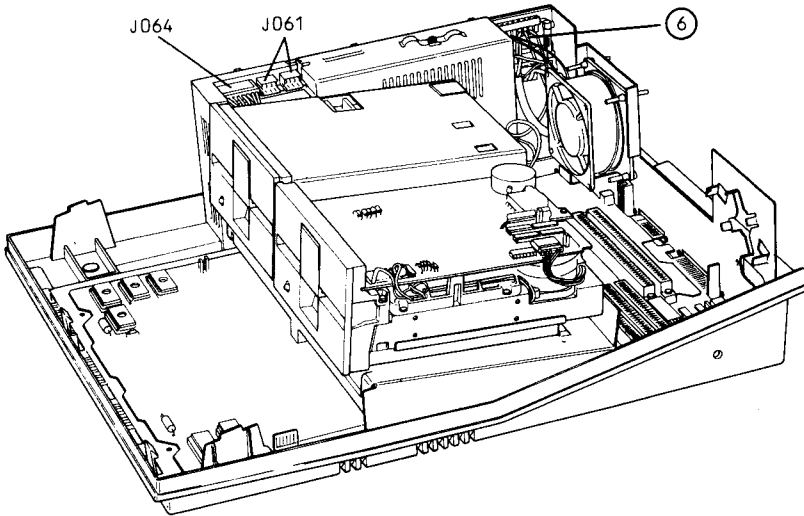


Fig. 3-17 Removal of Power Supply

3.3.5 REPLACEMENT OF FUSE

The fuse is located at the rear of the power supply unit.

Tools Required: Screwdriver

- 1) Unplug the CRT Display and any printer that may be connected to the system.
- 2) Remove the Basic Module cover.
- 3) Remove the fuse from the fuse holder.

To reinstall the fuse perform the same operations in reverse.

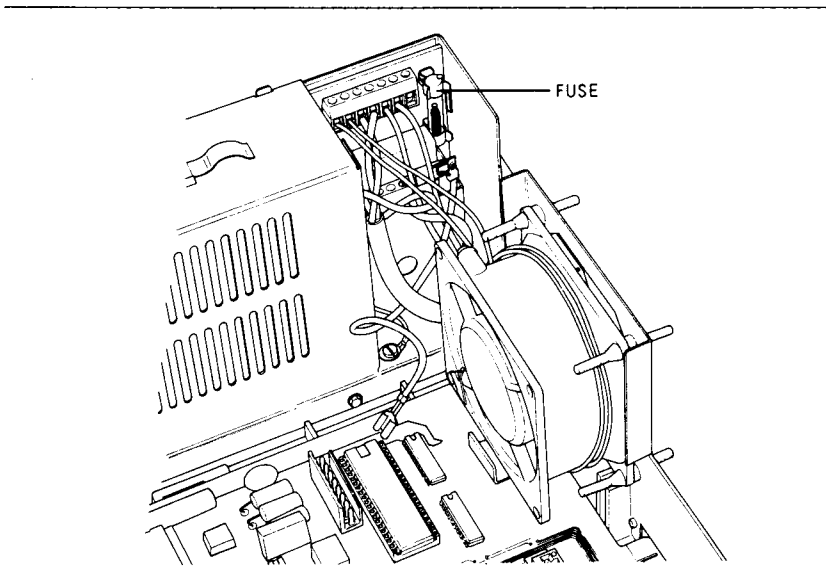


Fig. 3-18 Removal of Fuse

3.3.6 REPLACEMENT OF FAN

The fan is mounted on the appropriate block at the rear of the Basic Module by four plastic studs. Three wires connect the fan to the power supply.

Tools Required: Screwdrivers (Normal and Phillips)

1) Unplug the CRT Display and any printer that may be connected to the system from the Basic Module.

2) Remove the Basic Module cover.

3) Remove the wires which connect the power supply to the fan from the upper and lower terminal strips:

Earth wire (Green/Yellow) is disconnected from the lower terminal strip pin 3

One supply wire (black) is disconnected from the upper terminal strip pin 1

The other supply wire (black) is connected to the upper terminal strip pin 2

4) remove the plastic studs that fasten the fan the plate.

5) Remove the fan.

Reinstall the fan by performing the same operation in reverse.

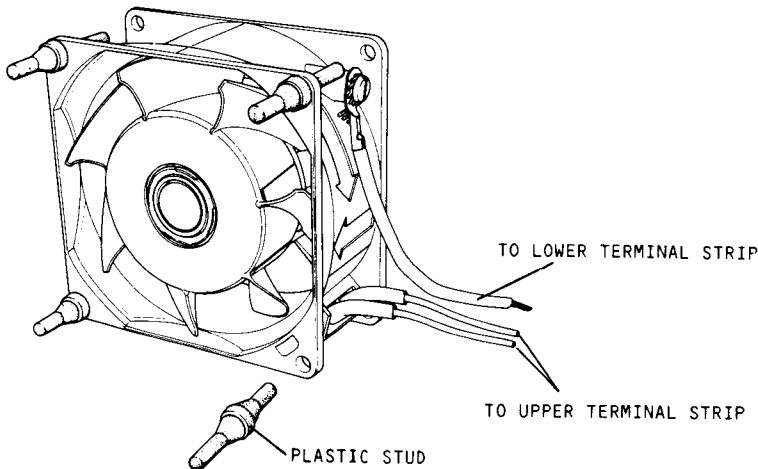


Fig. 3-19 Removal of Fan

3.3.7 REPLACEMENT OF MAINS POWER CABLE

The mains power cable is made up of three wires: Live (brown) fastened to the upper terminal strip pin 5
Neutral (blue) fastened to the upper terminal strip pin 4
Earth (yellow) fastened to the lower terminal strip pin 4

Tools Required: Screwdriver

Procedure for the removal of the mains power cable.

- 1) Unplug the CRT and any printer connected to the system from the Basic Module.
- 2) Remove the Basic Module cover, keyboard and front disk cover.
- 3) Loosen the three wires from the terminal strips
- 4) Slide the power supply unit forward until the cable clamp screws are accessible.
- 5) Loosen the two cable clamp screws.
- 6) Extract the cable from the Basic Module through the appropriate hole near the ON/OFF switch.

To reinstall the mains power cable perform the same operations in reverse.

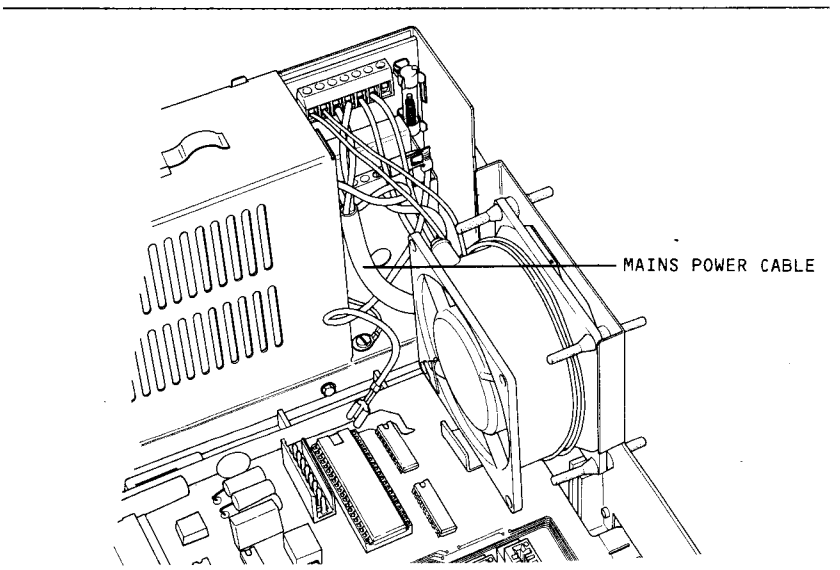


Fig. 3-20 Removal of Mains power Cable

3.3.8 REPLACEMENT OF MOTHERBOARD

The motherboard is the board that is found at the bottom of the Basic Module. Great care must be exercised in removing this logic board which contains all the logic circuitry.

Tools Required: Screwdriver

- 1) Unplug the CRT display and any printer that may be connected to the system from the Basic Module.
- 2) Remove the Basic module cover.
- 3) Remove any expansion memory boards or option boards plugged into the motherboard.
- 4) Unplug from connector J1 on the motherboard the cable that connects the power supply to the motherboard.
- 5) Remove the keyboard and front disk cover
- 6) Remove the mini-floppy disk drive(s) and associated cables.
- 7) Gently remove the motherboard by disengaging it from the mounting studs that run around the perimeter of the Basic module bottom.

Reinstall the motherboard by performing the same operations in reverse.

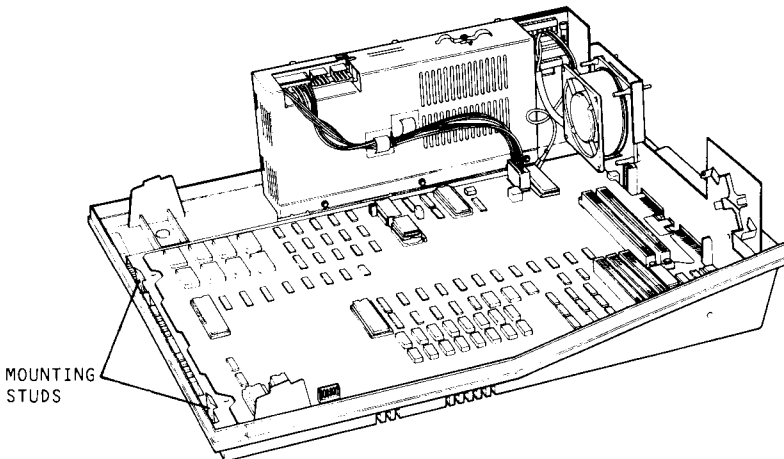


Fig. 3-21 Removal of Motherboard

3.3.9 REMOVAL OF KEYMODULE FROM KEYBOARD

The keyboard contains 74 keys, each with its own keytop and keymodule. The keyboard is connected to the motherboard by means of a cable that fits into connector J11 on the motherboard.

Tools Required: Screwdriver, 5mm + 5.5mm Tub Spanner

- 1) Unplug the CRT Display and any printer that may be connected to the system from the Basic Module.
- 2) Remove the Basic Module cover.
- 3) Remove the keyboard
- 4) Remove the yellow 'shift' keytop, the keytop alongside, and the second keytop of the row above. The keytops are easily removed by just pulling them towards the top.
- 5) Remove the Light Emitting Diode (LED) from the keyboard towards the top.
- 6) Loosen the two hexagonal nuts.
- 7) Lift the keyboard printed circuit board.
- 8) Remove the keytop of the keymodule to be replaced. The keymodule is then easily removed.

Note: Ensure that the keyboard signal wires are correctly soldered to the keyboard printed circuit board prior to reinstalling it.

Reinstall the keymodule by performing the same operations in reverse.

KEYTOPS TO BE REMOVED

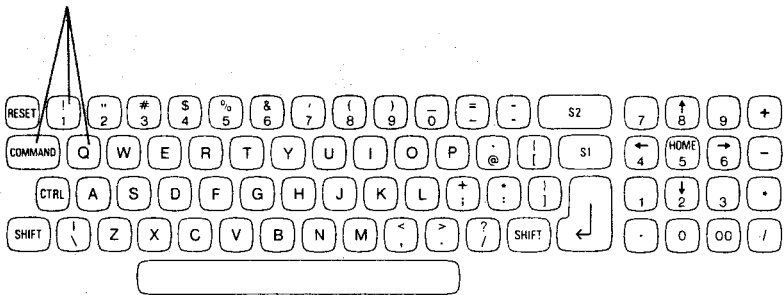


Fig. 3-22 Removal of keymodule

3.3.10 REMOVAL OF ON/OFF SWITCH

The ON/OFF switch is located at the rear of the Basic Module and is housed in the power supply unit.

Tools Required: Screwdriver

- 1) Unplug the CRT Display and any printer that may be connected to the system from the Basic Module.
- 2) Remove the Basic Module cover.
- 3) Remove the four wires of the ON/OFF switch that fit into the upper terminal pins 3, 4, 5, 6 of the power supply.
- 4) Remove the ON/OFF switch.

Reinstall the ON/OFF switch by performing the same operations in reverse.

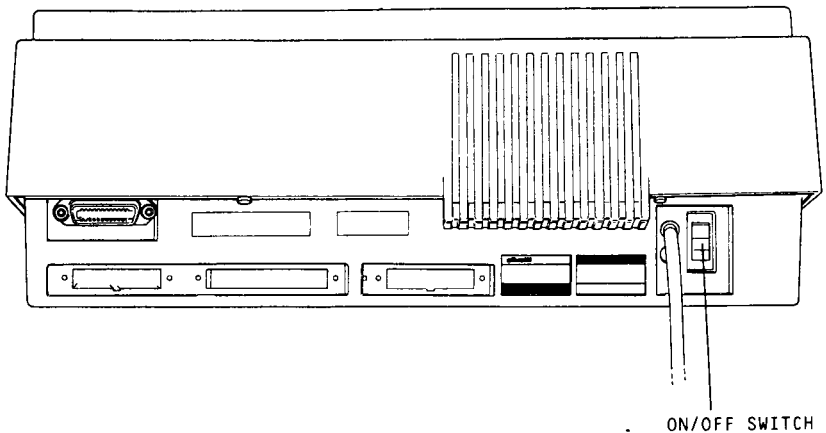


Fig. 3-23 Removal of ON/OFF Switch

3.3.11 REMOVAL OF CRT DISPLAY

Tools Required: Screwdriver, Allen Key

- 1) Unplug the CRT Display from the system.
- 2) Loosen the two screws located at the top of the CRT Display cover to the right of the brightness potentiometer.
- 3) Loosen the four allen screws at the bottom of the CRT Display cover.
- 4) Gently remove the CRT display cover.

To reinstall the CRT Display cover perform the same operations in reverse.

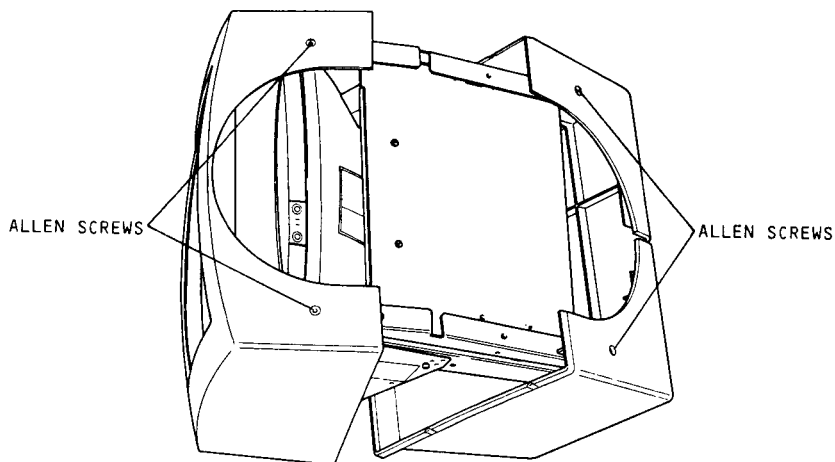


Fig. 3-24 Removal of CRT Display cover

POWER-UP DIAGNOSTICS

4. POWER-UP DIAGNOSTICS

4.1 INTRODUCTION

The power up diagnostics are executed each time the M20 is powered up or physical reset. These programs are resident in ROM and test the basic functionality of the various modules within the M20. The purpose of these programs is to assure a minimum working level of all the main modules in the M20. In order to execute these programs the basic CPU, clock, power supply, address and data paths must be operating correctly.

In general, the level of fault isolation is to the module level. For example, the keyboard and disk drive error messages point the user to the faulty module and are limited in scope, whereas the error messages associated with the testing of the RAMs, ROMs, and the remainder of the large scale integration (LSI) chips specify the faulty component.

4.2 TEST DESCRIPTION AND OPERATING PROCEDURES

The power up diagnostics run automatically every time the power switch is switched on or the reset button is pushed. During the power up sequence, a series of characters appear in the upper left corner of the display. Make sure the Brightness Control is properly set to get the best character definition. These characters indicate that certain internal functions have been tested and are functioning properly. At some stage the screen is filled with various patterns. This occurs during the RAM test. When all the tests have been verified the display shows:
Bootstrap Loader Rev. X.X

The M20 is now ready to process or run programs.
If on switching on, or on pressing the reset button, no diskette is present in the disk drive the following message appears on the Display:
Bootstrap Loader Rev. X.X
Insert diskette and type return.

If on switching on, or on pressing the reset button, the incorrect diskette is present in any of the drives the following message appears on the Display:
Bootstrap Loader Rev. X.X
Invalid File Error XX on Drive X.
Insert diskette and type return.

If the display does not show the previous information press the RESET

button. If the correct information is still not displayed consult section 4.3.

Three special functions may be invoked by pressing specific keys on the keyboard while the diagnostics are running. Pressing the 'l' key causes the diagnostics to enter a loop mode on all diagnostic tests. Status and error information are also sent to the parallel port. To exit loop mode press any key other than 'l',

Pressing the 'd' key causes the diagnostics to enter a loop mode which continuously reads side zero, track 16 of the first ready disk drive. If the disk drive configuration includes the hard disk unit (10), it is tested in loop mode. Otherwise, the first floppy disk drive (0) is tested in loop mode. If the first drive (0) is not ready (e.g. no diskette inserted), the diagnostic test attempts to read the same track on the second drive (1). If the second drive (1) is not ready (e.g. absent from disk drive configuration or no diskette inserted), the test loops back and continues to loop still looking for a drive that is ready. Once a ready drive is found, the diagnostic enters a loop which continuously reads side zero, track 16 of the ready disk.

Pressing the 'f' key causes the bootstrap loader to first attempt the bootstrap from the floppy disks before attempting the bootstrap from the hard disk. The normal sequence is to bootstrap from the hard disk first. Any other key that is detected as being pressed is saved and passed along to the operating system.

4.2.1 Z8001 CPU TEST

All registers (excluding the refresh counter) are checked to verify that all bits can be set zero and one.

All eight of the Z8001 CPU's addressing modes are checked: Register, Immediate, Indirect register, Direct Address, Index, Relative Address, Base Address, and Base Index.

The following instruction classes are tested with commonly used instructions from each class of the Z8001 CPU instruction set: Load and Exchange, Arithmetic, logical, Program Control, Bit Manipulation, Rotate and Shift, Block Transfer and String Manipulation, Input and Output, and CPU control.

The following modes of operation are tested: system, normal, segmented and non-segmented.

After the RAM and ROM modules are verified, the call instruction and the following traps are tested: vectored interrupt, non-vectored interrupt, system call, and privileged instructions.

After the real-time clock and keyboard have been initialized and tested handshake interrupts are tested on the real-time clock and keyboard.

4.2.2 ROM MODULE TEST

During this test the CPU calculates for each ROM chip a checksum. The

checksum should equal to the known value.

4.2.3 RAM MODULE TEST

This test is a limited test to verify that the RAM module is functional. First, each 16 kbyte RAM bank is checked to see whether its bank number can be written into and read from its last byte. Next, each word of every RAM bank has its own address written into it. The contents are then read and verified against the address. Then, the complement of the address is written each word. Again, the contents are read and verified against the address. Finally each RAM bank is completely filled with a fixed pattern of 1's, then read and verified. Similarly each RAM bank is first filled with a fixed pattern of 0's, and then tested. Thus, data integrity and some immunity to noise is verified. Also, the operations of multiplexing addresses to each RAM chip and demultiplexing them within each RAM chip are verified.

4.2.4 LSI CHIP TESTS

This test tests the basic functionality of the following integrated circuits: both 8251 USARTs, 8253 Timer, 8255 Parallel I/O Chip, 6845 CRT Controller, 1797 Floppy disk controller. This test does not however check the output of these devices. This test does however verify that registers can be written to and read from. This test thus verifies the data path to the chips, the chip enable logic, and the basic functionality of the chip itself.

4.2.5 KEYBOARD TEST

To test the keyboard a command sequence is sent to the keyboard to cause the keyboard to enter a self test mode. The keyboard must respond within a certain period of time with the correct test responses. This test verifies the operation of the keyboard and the serial communication with the keyboard.

Then, the presence of a jumper on the keyboard communication link is tested here to determine whether a flag should be set to cause the system to loop on diagnostic testing upon completion of the current pass. Next, the keyboard country code is input from the keyboard and stored in memory to be used later on by the operating system. Finally a command is issued to the keyboard to generate a pair of audible signals to the user.

4.2.6 DISK DRIVE TEST

First, the ROM floppy disk driver is initialized and a determination is

made regarding the configuration of the disk drive hardware. A check is made to see if the hard disk unit (10) is present. If it is present, a command to read side zero track zero is issued. If this task can be performed without seek or data errors, then the hard disk drive unit subsystem is assumed to be functional. Next, regardless of whether the hard disk unit (10) is present, the first floppy disk drive (0) is checked for ready status. If the first drive (0) is ready, the test described above is performed on drive (0). Next, regardless of whether the first floppy disk drive (0) was ready, the second floppy disk drive (1) is checked for a ready status if it is present in the disk drive hardware configuration. If the second drive is present and ready, the test is repeated on drive (1). If the hard disk unit is absent from the particular hardware configuration, and neither floppy disk drive is ready, this test is skipped.

4.3 TEST PROGRAM FLOW

The following sequence (see also flow chart at end of chapter) is executed at the time of the power-up or when the hardware reset button is pressed:

1. The video controller chip (6845) is programmed. Only load, increment, output, and jump relative instructions are used.
2. The parallel printer port chip (8255) is programmed. Only load and output instructions are used.
3. Four bytes are written to the bitmap RAM that form a small triangle in the extreme upper left corner of the video display, signifying the beginning of the Z8001 CPU diagnostics.
4. The Z8001 CPU's registers, addressing modes, instruction classes, and modes of operation are tested. Testing the CPU's trap and call instruction capabilities is delayed until after the ROM and RAM modules have been tested. The interrupt diagnostics are postponed until after the real-time clock and the keyboard have been initialized and tested, because both are serviced as part of the test. If a failure is detected, the small TRIANGLE remains on the video display, and an infinite loop is entered.
5. The keyboard USART chip (8251) is programmed and initialized, so that the user is allowed to input from the keyboard.
6. Four bytes are written to the bitmap RAM so as to form a small SQUARE in the extreme upper left corner of the video display, signifying the beginning of the ROM module diagnostic tests.
7. The ROM module test is performed. If a failure is detected, the small SQUARE remains on the video display, an 'E Hn' or 'E Ln' error message is sent to the parallel printer port, and an infinite loop is entered.
8. Four bytes are written to the bitmap RAM so as to form a small DIAMOND in the extreme upper left corner of the display, signifying the beginning of the RAM module diagnostics.
9. The RAM module test is performed. If a failure is detected, the small DIAMOND remains on the video display, an 'E Mc bb ssss www' error message is sent to the parallel printer port, and an infinite loop is entered.
10. The Z8001 CPU trap and call instruction tests are performed. If an illegal trap error is detected here or earlier, four bytes are written to the bitmap RAM so as to form FOUR small vertical BARS in the extreme upper left corner of the video display, and an infinite loop is entered.

11. The screen driver, parallel printer port driver, and the real-time clock drivers are initialized. The real-time clock USART (8253) is initialized. The video display and the parallel printer port can now be safely used for displaying error messages.

12. The remaining of the large scale integration chips (LSI) are then tested. If a failure is detected, an 'E Cy' error is written on the video display, and execution of the diagnostics continues. The serial baud generator (8253) is programmed to provide a 1200 baud rate for the keyboard and a 9600 baud rate for the RS 232 serial port. Both USARTs (8251) are initialized at this point.

13. The keyboard USART (8251) is checked to see whether any other key has been struck. If a single key is pressed, the key is saved for later use.

14. The keyboard test is performed. A self test command is issued to the keyboard, which must be answered promptly and correctly. If the presence of a jumper on the keyboard communication link is detected here, the system sets a flag to loop on diagnostic testing. The country code sent by the keyboard is saved for later use by the operating system. If a failure is detected, an 'E Ky' error is written on the video display and execution of the diagnostic continues.

15. The Z8001 CPU's interrupt service procedure is tested using the real-time clock and the keyboard. If a failure is detected, an 'E ly' error is written on the video display, and an infinite loop is entered.

16. The disk driver is initialized, and the disk drive test is performed. Track 16, side zero is read on all ready disk drives in the particular hardware disk configuration. If the hard disk is absent and neither floppy disk drive is ready, this test is skipped. If a failure is detected on a ready drive, this test is skipped. If a failure is detected on a ready drive, an 'E Dy' error is written on the video display, and execution of the diagnostics continues. This marks the end of the actual diagnostic testing. Now, a decision is made as to where the program should branch depending on whether the user has struck a key on the keyboard.

17. If the 'd' key was pressed, this process enters a loop which continually reads side zero, track 16 on the first ready drive.

18. If the 'l' key was pressed (or the loopback jumper detected), the system enters a loop which continually runs the diagnostic software and prints the pass count and any error information passed to the parallel printer port.

19. Otherwise, control is transferred to the boot-strap loader which loads the operating system from the first ready disk drive. If the diskette containing the operating system has not been mounted on one of the disk drives at this point, a boot-strap error message prompts the user to:

"Insert system diskette and type any key"

20. Any key pressed other than a 'd', 'l', or 'f' along with the key-board country code is saved in RAM and passed along to the operating system.

4.4 ERROR MESSAGES AND TABLES AND INTERPRETATION

4.4.1 MESSAGE DISPATCHING

When an error is encountered in the power up diagnostics it is displayed on the CRT screen. However, if the video circuitry is not working, and the printer driver has already been initialized the error message is sent to the parallel printer port. Hence, by connecting a printer to the parallel port one can get some indication as to the type of error encountered by looking at the printout.

MESSAGE SYNTAX

SCREEN MESSAGE	PRINTER MESSAGE	COMMENTS
Triangle	None	Faulty CPU - CPU addressing Mode test or CPU instruction class test have failed.
Square	E xn x = H or L (High or Low byte) n = ROM number (1 to 4 inclusive)	ROM failure
Diamond	E Mc bb ssss www c=RAM config. number bb = bank failure no. ssss= data expected www= data read	Faulty RAM - If test stops abruptly while displaying patterns on screen, then very likely the RAM test has failed.
Four Vertical Bars	None	CPU call and trap tests have failed.
EC0	EC0	Faulty 8255 Chip
EC1	EC1	Faulty 6845 Chip
EC2	EC2	Faulty 1797 Chip
EC3	EC3	Faulty 8253 Chip
EC4	EC4	Faulty 8251 K/B Chip
EC5	EC5	Faulty 8251 RS 232 Chip
EC6	EC6	Faulty 8259 Chip
EK0	EK0	Keyboard error - No response
EK1	EK1	Keyboard Error - Self-test failure

SCREEN MESSAGE	PRINTER MESSAGE	COMMENTS
E10	E10	Interrupt Error - Non-vectorized interrupt
E11	E11	Interrupt Error - vectorized interrupt
ED0	ED0	Disk error drive 0
ED1	ED1	Disk Error drive 1
ED10	ED10	Disk Error drive 10 (Hard Disk Drive)

A small diamond appearing in the extreme upper left corner of the video display, indicates a failure in the RAM diagnostics. An error message is sent to the parallel port with the following format:

E Mc bb ssss wwww

where:

c = RAM configuration number (hardware configuration number of the particular M20 system)

Configuration 3 = M20 with at least one 32KB memory expansion board

bb = Bank failure number

The following table cross references the bank number against the actual physical location of the memory.

BANK NUMBER	PHYSICAL LOCATION
Bank 00	Motherboard
Bank 04	Motherboard
Bank 05	Motherboard
Bank 06	Motherboard
Bank 09	Motherboard
Bank 0A	Motherboard
Bank 01	First Expansion Board
Bank 07	First Expansion Board
Bank 0B	First Expansion Board
Bank 02	Second Expansion Board
Bank 03	Third Expansion Board
Bank 11	Third Expansion Board
Bank 12	Third Expansion Board

ssss = What data should be

wwww = What data was read

All the above is best illustrated by an example. If the printer on power-up prints the following:

E M3 01 4000 C000

System with configuration number 3 and error occurred in bank 01 i.e. in FIRST EXPANSION BOARD.

Data should be: 0100 0000 0000 0000

Data read was: 1100 0000 0000 0000

Faulty bit is the lefthand most one i.e. D15. Looking at the schematics of the B/W 32KB expansion board we see that U7 is the faulty RAM chip.

BOOTSTRAP ERROR MESSAGES

While the boot-strap loader is executing, several different error messages can occur. If neither of the floppy disk drives is READY, the following error message appears on the video display:

Insert system disk and type any key

Insert the diskette containing the PCOS operating system and depress any key. If the file pointed to by the "pcos_fdb" pointer on block zero of

any disk is not properly formatted for boot-strap loading, the following error message appears on the video display:

Invalid Boot Fil: xx

where xx = 00 implies an invalid extent count for the file descriptor block.

xx = 01 implies invalid file type

xx = 02 implies an invalid block count

xx = 03 implies an end-of-file error

xx = 04 implies parameter is out of range for disk drive

During the boot-strap process, if a disk error occurs, the following error message appears on the video display:

Disk Error: xx

where xx is the 2 digit hexadecimal display of the floppy disk driver return code.

The floppy disk driver return code is a single byte. Its eight bits have the following meaning:

bit 7 : Drive not ready error (most significant bit)

bit 6 : Write Protect Error (Bad block error for hard disk)

bit 5 : Write Fault error

bit 4 : Record not found error

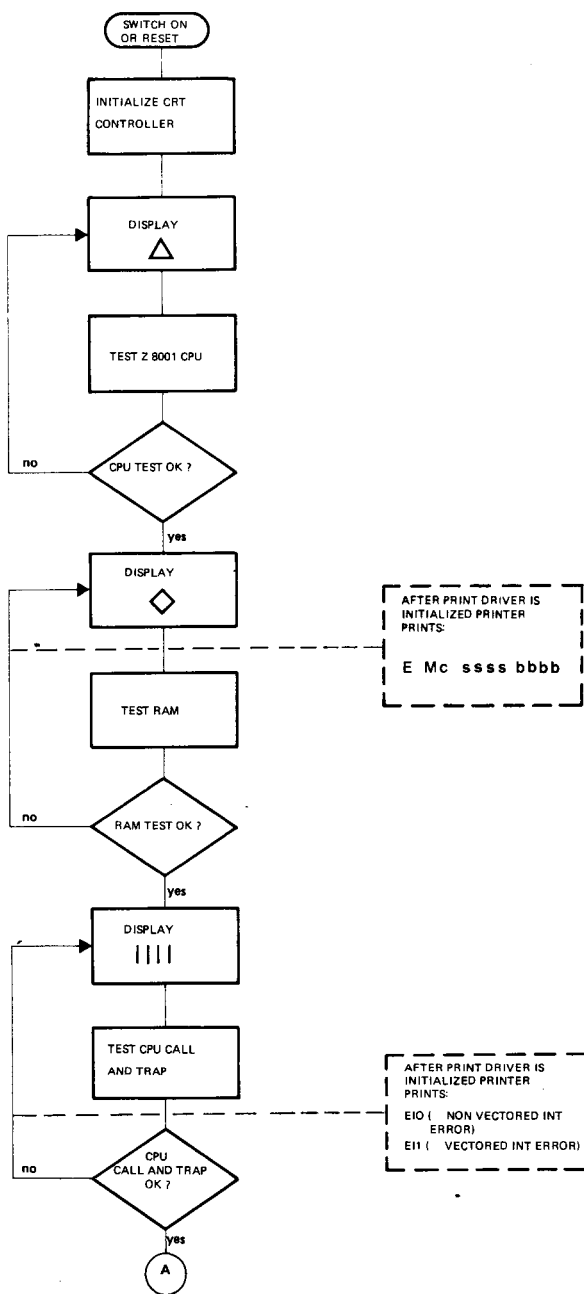
bit 3 : Data transfer error

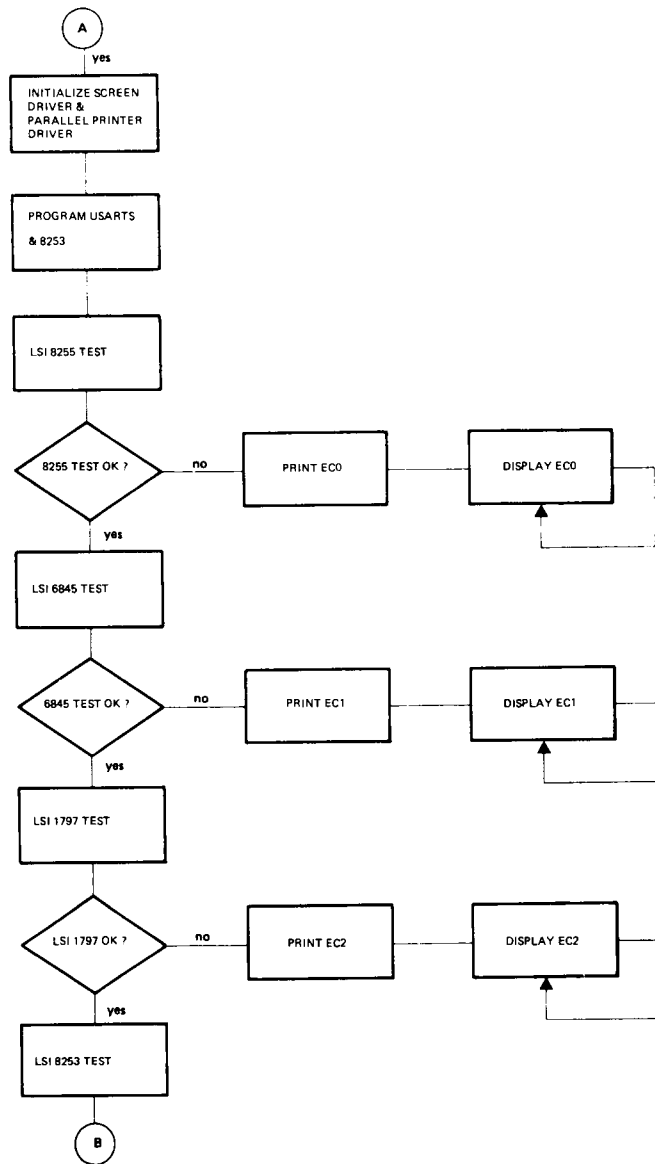
bit 2 : Seek error

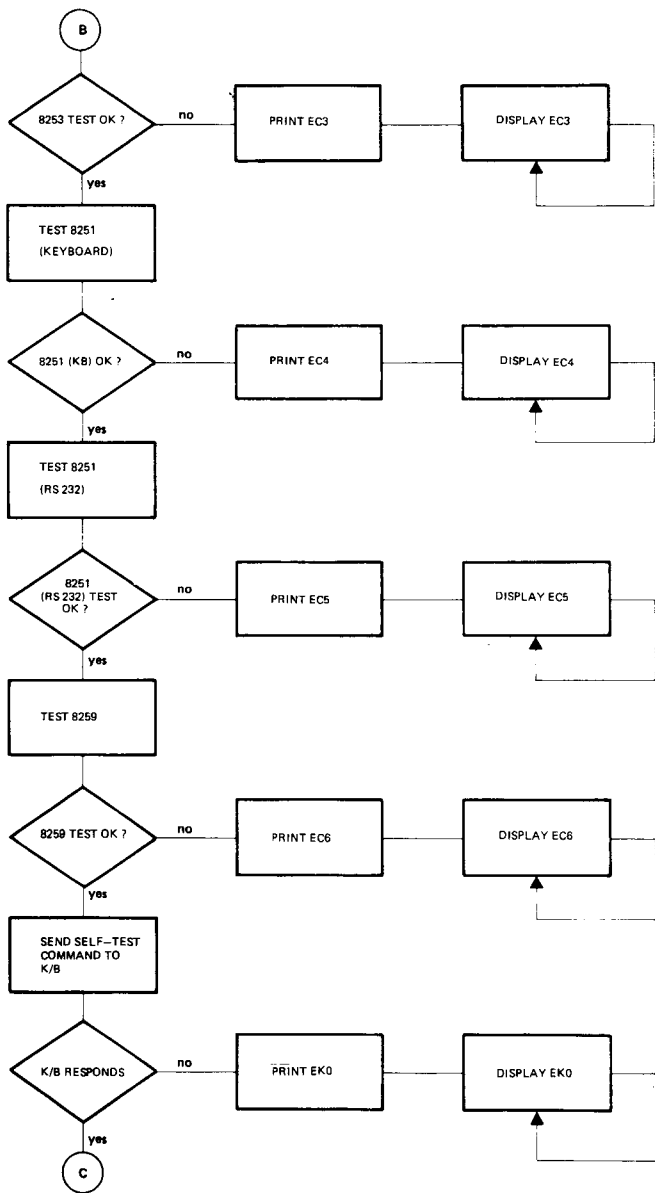
bit 1 : After restore, Not Track zero

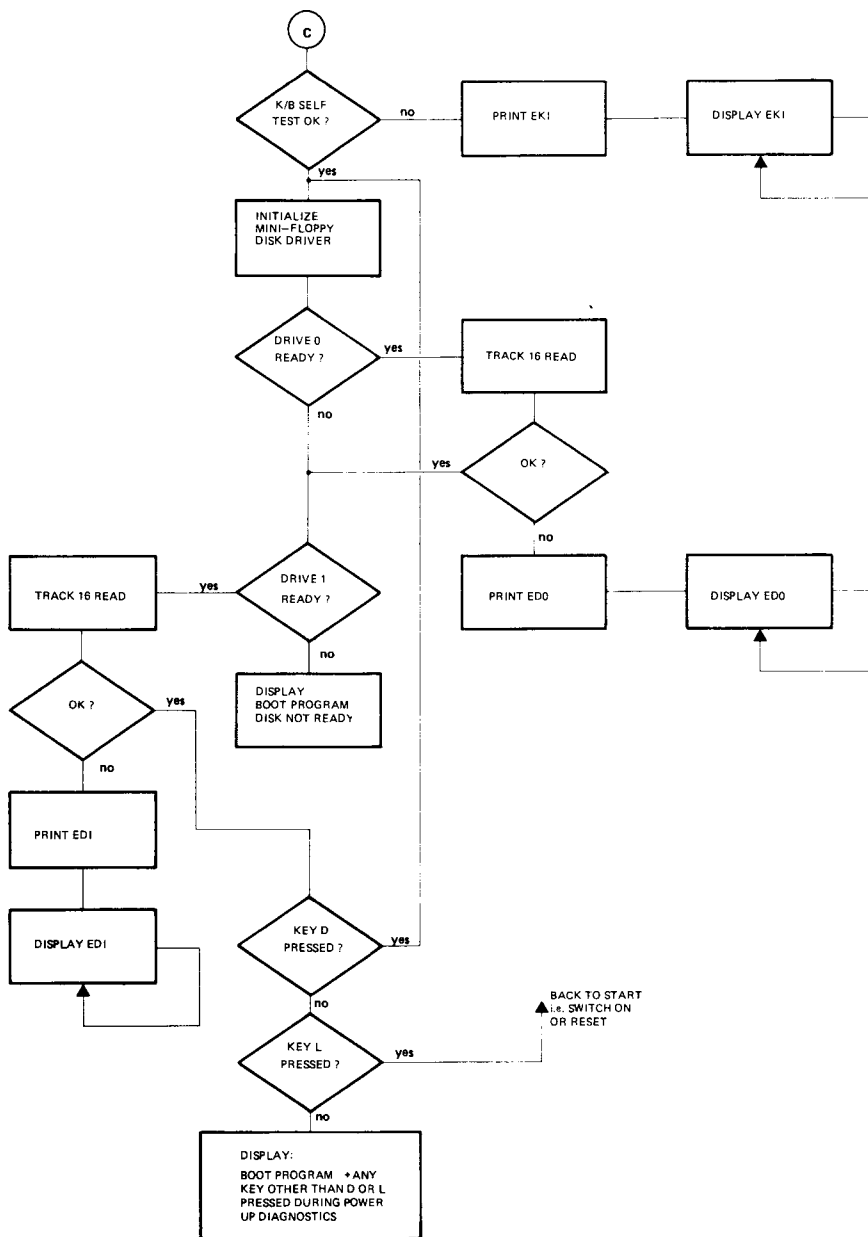
bit 0 : Illegal Parameters (least significant bit)

Several of these bits can be set, signifying more than one error.









5

OLITEST

5. OLITEST

5.1 INTRODUCTION

The user diagnostics are loaded via a special diagnostic disk supplied to the user. The Olivetti commercial name for this diagnostic disk is OLL-TEST. The purpose of OLITEST is to provide the user with a set of tests to verify the functionality of the M20 modules. The tests are disk based and can be selected individually as needed. These comprehensive tests include a keyboard test, video module test, a mini-floppy disk test, a motherboard test, an RS 232C Interface test, a parallel interface test, and an IEEE 488 Interface test. These tests allow the user to gain a degree of confidence in the correct operation of the system as well as teach him to discriminate between hardware and software problems. These tests allow the user to relate more information when communicating with the field service personnel. Field service personnel should always carry out the user diagnostics in order to verify and confirm the user's complaint. In many cases, it is necessary and advisable for the field service personnel to carry on with the System test in order to confirm their diagnosis.

5.2 OPERATING PROCEDURES

The Olitest disk, when inserted into the M20 automatically bootstraps the test executive. The Olitest is executed by placing the disk in either the right or left hand drive and resetting the system (this may be either a physical reset or a keyboard reset). A menu of all the possible tests is then displayed:

- Video Display test
- Keyboard Test
- Motherboard Test
- Mini-Floppy Disk Test
- RS 232C Test
- Parallel Interface Test
- IEEE Interface Test
- Quit

The Olitest diagnostics are self prompting. All the commands are listed on the screen. The tests are selected by positioning the cursor next to

the desired test. The cursor is moved by using the cursor keys, only the cursor up and cursor down keys are used (the "2" and "8" on the keypad). When the cursor is next to the desired test the return key is pressed. This prints a short description of the test. Next the user is asked if he wants the test to run. If he decides he does not want the test to run he enters "n" and the main menu is displayed. If he wants to run the test he presses "y" and he is asked how many times he wants to run the test. He then enters a number between 0 and 999. This test is executed this number of times. If an error occurs then an error code is displayed and the test stops. The user may get back to the main menu by pressing the key "S2". If the tests finish with no errors the operator may select to either run the test again or go back to the main menu.

5.2.1 VIDEO DISPLAY TEST

After selecting this test the following test menu appears on the Display:

```
Colour Pattern test
Graphic Pattern
Character Set
Return to Main Menu
```

The tests are selected by positioning the cursor next to the desired test and pressing the return key. The cursor is moved by using the cursor keys, only the cursor up or down keys are used (the "2" and "8") on the keypad.

The user may get back to the main menu by positioning the cursor next to "Return to Main Menu" command and then pressing carriage return.

5.2.2 KEYBOARD TEST

After selecting this test, a description of the keyboard test appears on the screen. this test first executes the keyboard self test. If the self test is succesful, the user is asked whether he wants to continue with the keyboard test. If the user presses "y", then a picture is drawn on the screen with all the keys shown as they appear on the users keyboard. The user now presses the key indicated by the blinking cursor. If the shift, control or command keys are being tested then the shift, control or command key is painted white along with the blinking cursor on the other key. For example, if CONTROL A is being tested then the control key is painted white and the A key has the cursor blinking. The user goes on to test the next section by pressing "S2". When the test is finished all keys which were found bad are displayed. Each key is checked three times before it is considered bad. When the keyboard test is completed all errors are listed.

5.2.3 MOTHERBOARD TEST

After selecting this test, a short description of the test appears on the screen. The user is then asked whether he wants to run the test. If he answers "y", then he is further asked how many times he wants to run the test. After inputting a valid number (between 0 and 999) the motherboard test starts running. The user does not see it running but only sees the message "Motherboard Test Running". If the test is successful, the user is asked whether he wants to run the test again or return to the main menu. The user may stop the test at any time by pressing "S2" and returning to the main menu. If an error occurs then an error code is displayed and the test stops.

5.2.4 MINI-FLOPPY DISK TEST

After this test is selected, a brief description of the test appears on the screen. The user is then asked whether he wants to continue with the test or not. If he answers "y", then he is asked to input which disk drives he wants to test: either drive 0 (right hand drive), drive 1 (left hand drive), or the hard disk drive (10). The user can test any combination of drives by typing in the drive numbers. For example, if the operator wants to test the hard disk drive and drive zero he enters: 0,10 or 10,0. All types of drives are tested: 160KB, 320KB, 640KB and hard disks. He is then requested to place blank formatted disk in the appropriate drives. The test is now executed and takes approximately 2 minutes to execute.

5.2.5 RS 232C INTERFACE TEST

After this test is selected, a brief description of the test appears on the Display. This test checks the serial port on the motherboard and if present the TWIN RS 232C option. This test requires that a loopback jumper be connected to the serial port, and if the TWIN RS 232C board is present it also requires a jumper. (see section 4.5 for loopback jumpers construction). The user is then asked whether he wants to continue with the test or not. If the answer is "y", the user is then asked how many times he wants to run the test. To stop the test at any time the user presses "S2".

5.2.6 PARALLEL INTERFACE TEST

After this test is selected, a brief description of the test appears on the screen. The user is then asked to insert a loopback jumper in the parallel port on the motherboard. (see section 4.5 for loopback jumpers construction). The user is then asked whether he wants to continue with this test or no.

If the answer is "y", then the user is asked how many times he wants to run the test.
The user may stop this test any time by pressing the key "S2".

5.2.7 IEEE 488 INTERFACE TEST

After this test is selected, a brief description of the test appears on the screen. The user is then asked whether he wants to continue with this test or no. If the answer is "y", then the user is asked how many times he wants to run the test. The user may stop the test at any time by pressing "S2".

5.3 TEST DESCRIPTIONS

5.3.1 VIDEO TESTS

The video tests are used to verify the operation of the video controller and the Display unit itself. These tests operate in both colour and black and white.

5.3.1.1 Colour Pattern Test

This test is mainly used to check the different colours on the M20. The test first draws a pattern and then colours it in. If this test is run on a black and white M20 then this pattern is not coloured in. Next the eight different colours are displayed, one at a time with their names. If this test is run on a black and white system only black and white is displayed.

5.3.1.2 Graphic Pattern

This section displays a pattern on the screen which allows the Display unit itself to be adjusted.

5.3.1.3 Character Set

This section displays the full M20 character set in both normal and reverse video.

5.3.2 KEYBOARD TEST

The purpose of this test is to determine if all of the mechanical switches, the electronics and bell functions are working properly. The electronics of the keyboard are tested using the same self test mode of the keyboard during power up diagnostics. Each key is checked three times before it is considered bad.

5.3.3 MOTHERBOARD TEST

This test checks the following areas of the motherboard:

- Memory (including first expansion board)
- Large Scale Integration Chips (LSI)
- CPU

5.3.3.1 Memory Test

This tests the RAM memory and includes 7 separate tests which are executed sequentially. The default number of times these tests are run is five times. The following is a description of the seven tests: Bank Select Test

This test writes into each 16K bank its bank number. the test then verifies that each bank contains its bank number. This test also verifies the correct operation of the bipolar mapping ROM, and all the chip select logic to the RAM memory devices.

Fixed Pattern Test

This test writes to each memory location the current test pattern and immediately verifies the pattern. The test cycles through all of the memory twenty four times, using a different pattern each time. The twenty four patterns in hexadecimal format are: FFFF, 0000, 5555, 0101, 0202, 0404, 0808, 1010, 2020, 4040, 8080, FEFE, FDFD, FBFB, F7F7, EFEF, DFDF, 8F8F, 7F7F, FF00, 00FF, AA55, 55AA.

Address Test

This test writes into each memory location its address. The memory is then checked to verify the addresses. This test is done using byte operations so that it can first be done using even addresses and then using odd addresses. The test is then repeated writing the complement of the address into memory location. Thus all of the memory is written and read four times in this test.

Marching Test

The same twenty four fixed patterns used in the fixed pattern test are used in this test. The memory is first filled with the first pattern. Starting at the beginning of memory the pattern is read and verified, and then the complement of the pattern is written into the cell and verified. The test then goes to the next cell and repeats the same process until the end of memory is reached. When the end of memory is reached the test

starts backwards verifying the pattern, complementing it, storing it, and verifying it. This is repeated for each cell until the beginning location is reached. This process is repeated for all 24 patterns. All of memory is written and read 96 times in this test.

Buss Noise Test

This test uses two unique instructions of the Z8001 CPU to exercise the memory, address and data busses. The test fills the memory with a pattern using the LDIR (Load, Increment and Repeat) instruction. Memory is then checked using the CPIR (Compare, Increment and Repeat) instruction. This is repeated using all 24 fixed patterns. This entire sequence is then repeated 8 times. all of memory is written and read 192 times.

Moving inversion Test

This test uses a complex algorithm in which a field of zero bits is inverted and then reinverted again with each pass. This process is repeated using address steps which with each pass are multiplied by two. This test is run first with a forward sequence and then a backward sequence. Several main characteristics of this algorithm are that each write is written between two read actions, and that the addresses are generated in different increments and directions.

Refresh Test

This test first writes a zero pattern to all blanks under test. The test then delays 10 seconds and verifies that all memory locations still contain the zero pattern. This is repeated using an FFFF pattern. This test verifies that the RAM memory is being correctly refreshed by the video display circuitry.

5.3.3.2 CPU Test

This test is an exhaustive test of the CPU chip. All of the addressing modes and instruction classes performed in the power-up diagnostics are tested again in a more complete manner. That is, using many different registers in the different modes.

A test of the CPU registers is performed. This test checks each register for storage ability and pattern sensitivity. This is accomplished by testing with many different fixed patterns, using shifts and rotates, loads and exchanges.

5.3.3.3 LSI Chip Test

This test tests the functionality of the following integrated circuits: both 8251 USARTs, 8253 Timer, 8255 Parallel I/O Chip, 6845 CRT controller, 1797 Floppy Disk Controller. Various registers are tested as well as the chip enable logic and the data path to the chips.

5.3.4 MINI-FLOPPY DISK TEST

This test enables the user to verify the correct operation of one or two

disk drives present as well as the disk interface. This test works with any disk that has some free space remaining, although it is best to use a blank formatted disk. Each pass takes approximately 2 minutes per drive to execute. This test writes a random buffer to the entire disk and then verifies it.

5.3.5 RS 232C INTERFACE TEST

This test, as explained before requires a jumper to be connected to the RS 232C serial port connector. This jumper connector (STAC code: 57841Y) is the same used for System Test and Codia. This jumper connects the following signals: RXD to TXD; RTS to CTS; DSR to DTR; and CLKOUT to CLKIN. This jumper allows complete testing of the RS 232C interface.

The test program first verifies the correct operation of the handshake lines by placing data patterns on the DTR output line, and then reading the DSR status bit. This verifies the DSR and DTR functions within the USART and the buffers. The RTS is then made inactive and an attempt is made to send and receive data. If the RTS output and CTS inputs are working properly, no data should be received. The RTS is then made active and the attempt is made again. This time the data should be received. This verifies correct operation of the RTS and CTS functions of the USART and the line buffer and receiver.

The TXD and RXD and associated buffer and receiver are tested by sending out streams of various data and checking to make sure they are received. This test also tests the TWIN RS 232C board if it is present. It in fact checks either the RS 232C or current loop options.

5.3.6 PARALLEL INTERFACE TEST

This test requires the jumper to be connected to the parallel port connector. The jumper connects the A port (outputs) to the B ports (inputs), and then connects various handshake signals used on port C. The test writes all 256 binary patterns to the output port and reads the input port after each output to verify correct operation. The handshake signals (strobe and acknowledge) are tested using the set and reset bit functions of the 8255 chip.

5.3.7 IEEE 488 INTERFACE TEST

This test does not require any jumpers to be installed and checks the main components of the IEEE 488 interface:

- Controller Circuit (8292)
- Talker/Listener (8291A)
- Interface Circuitry (8293)
- Interrupt Circuitry

5.4 ERROR MESSAGES

5.4.1 VIDEO ALIGNMENT TEST

No errors are displayed since this test relies entirely on the user to determine if the Display is correct and aligned properly.

5.4.2 KEYBOARD TEST

No error codes are displayed in this test. If the keyboard self test fails then a message is displayed saying that the keyboard test has failed. The remainder of the test notifies the operator if any keycodes are received. When the keyboard test is completed all errors are listed.

5.4.3 MOTHERBOARD TEST

The following error codes are displayed:

Error -256	Error on Motherboard
Error 256	Error on RAM Expansion Board
Error 1	8255 Chip Error
Error 2	6845 Chip Error
Error 3	1797 Chip Error
Error 4	8253 Chip Error
Error 5	RS 232C 8251 Chip Error
Error 6	Keyboard 8251 Error
Error 7	8259 Chip Error
Error 8	Z8001 CPU Error

5.4.4 MINI-FLOPPY DISK TEST

The following errors are displayed:

Error 51	Data read from disk incorrect
Error 57	Disk I/O Error

5.4.5 RS 232C ERROR

The following errors are displayed:

Error 2	Motherboard Serial Port Failure
Error 4	Twin RS 232C port 0 Error
Error 8	Twin RS 232C port 1 Error

5.4.6 PARALLEL INTERFACE ERROR

The following errors are displayed:

Error 1 Port A to Port B Error
Error 2 PC5 Error
Error 3 PC4 Error

5.4.7 IEEE 488 INTERFACE TEST

The following errors are displayed:

Error -1 No Board present
Error 1 8259A Chip Error
Error 2 8291A Chip Error
Error 3 8292 Chip Error

5.5 JUMPERS

5.5.1 SERIAL TEST

The following jumper is required for the motherboard RS 232C test (same as System Test). It must be installed on motherboard connector J7.

NAME	PIN	TO	PIN	NAME
TXD	2	-	1	RXD
CTS	6	-	5	RTS
DTR	4	-	3	DSR
DTR	4	-	10	RING DETECT
DTR	4	-	12	SIGNAL DETECT
TXC-	16	-	13	RXCLOCKIN
LOCKOUT				

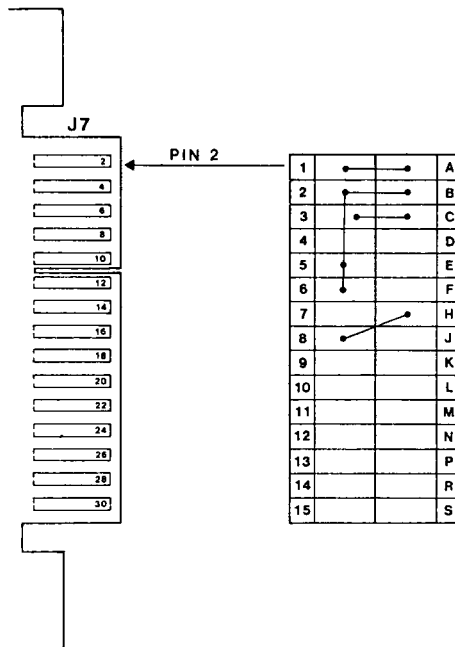


Fig. 5-1 Motherboard Serial Jumper

The following jumper must be installed on J35 if the TWIN RS 232C Board is present:
 RS 232C Mode

NAME	PIN	TO	PIN	NAME
TXD01	5	-	11	RXD01
TXD02	26	-	32	RXD02
CTS01	12	-	3	Ground
CTS02	29	-	3	Ground

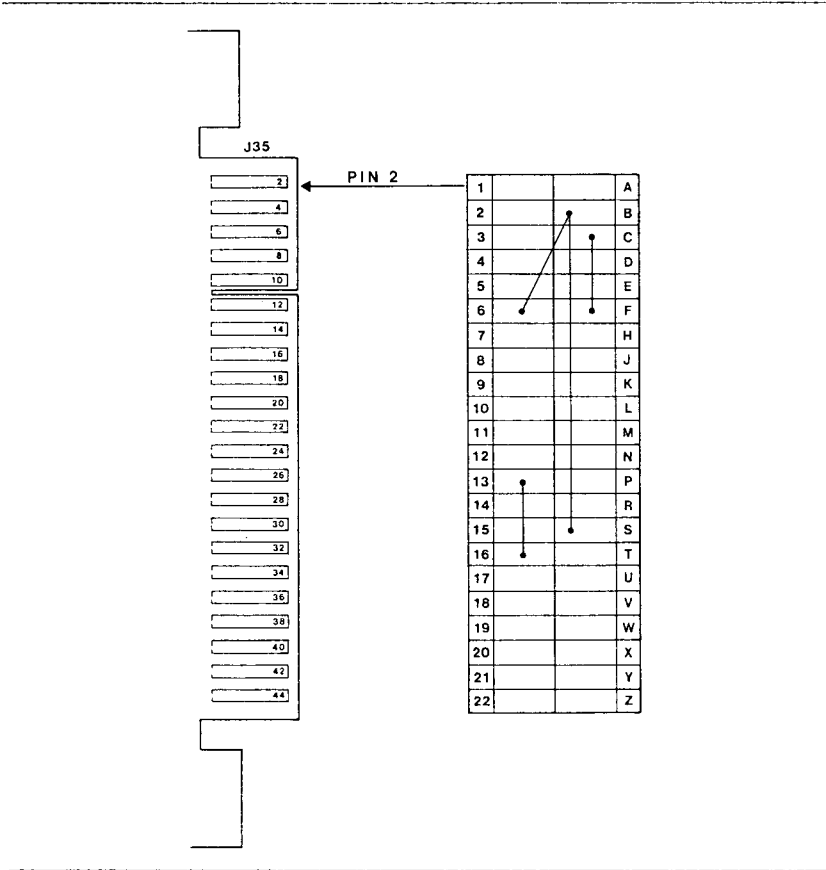


Fig. 5-2 RS 232C Loopback Jumper

Current Loop Mode

NAME	PIN	T0	PIN	NAME
LPSL1	6	-	3	Ground
LPSL2	23	-	3	Ground
TCL01	18	-	20	RCL01
TCL02	17	-	19	RCL02
TCL03	35	-	37	RCL03
TCL04	38	-	40	RCL04

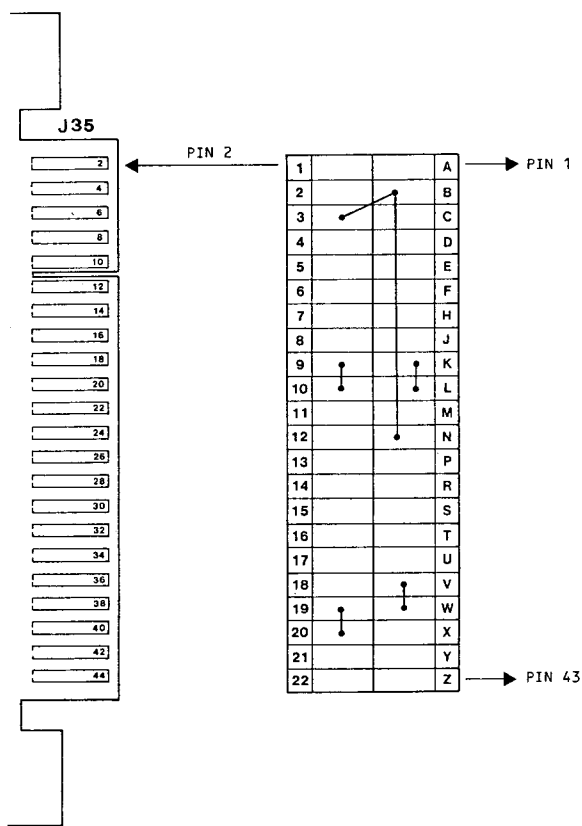


Fig. 5-3 Current Loop Loopback Connector

5.5.2 PARALLEL TEST

The following jumper must be installed on the motherboard parallel connector J6 (same as System Test):

NAME	PIN	TO	PIN	NAME
PA0	4	-	32	PB0
PA1	6	-	22	PB1
PA2	8	-	30	PB2
PA3	10	-	24	PB3
PA4	12	-	26	PB4
PA5	14	-	28	PB5
PA6	16	-	34	PB6
PA7	18	-	36	PB7
PC5	2	-	20	PC6

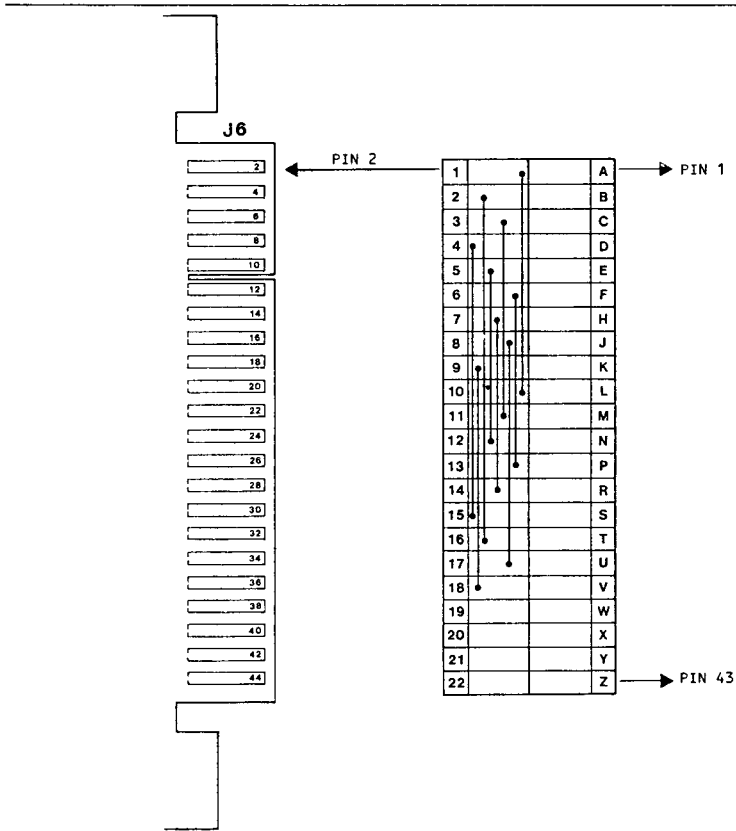


Fig. 5-4 Parallel Loopback Jumper

6

SYSTEM TEST

6. SYSTEM TEST

6.1 INTRODUCTION

The System Test comprises a series of tests resident on diskette and loaded into RAM memory. There are three System Test diskettes. The first contains all the major tests, the second contains only the Hard Disk test, and the third contains the tests for the Twin RS 232C board. Sections 6.2 to 6.4 deal with the first System Test diskette. It contains all the tests for the major M20 modules (CPU test, Memory test, Video test, LSI tests, Keyboard test, Min-Floppy Disk test, RS 232C interface test, Parallel Interface test, Parallel printer test). This diskette is used by the field engineer for functional verification of the M20 system following repair as well as for alignment of the various modules. This diskette is also used by the Olivetti Manufacturing and Quality Assurance Organizations. This test runs with the PCOS Operating System hardware drivers. Along with the test programs, diagnostics are also provided to allow fault isolation of a failing system.

6.2 OPERATING PROCEDURES

The system test diskette, when inserted into the M20 system automatically bootstraps the test executive.

SHOULD THE SYSTEM TEST FAIL TO LOAD BECAUSE OF A BLOCKING ERROR IN THE POWER-UP DIAGNOSTICS, THEN THE OPERATOR HAS TO GROUND U11 PIN 8 ON MOTHERBOARDS OF LEVEL "CP2" AND PUT JUMPER ZA IN POSITION ZA-1 ON MOTHERBOARDS OF LEVEL "D4" AND ONWARDS. THE SYSTEM TEST WILL THEN BE LOADED AND BYPASS SOME BLOCKING ERRORS.

The error logging option is then displayed. The operator has the option of choosing whether :

- a) the errors are to be displayed on the CRT Display only
- b) the errors are to be displayed on the CRT Display and also printed on the serial printer
- c) the errors are to be displayed on the CRT Display and also printed on the parallel printer
- d) the errors are to be displayed on the CRT Display and logged to the diskette in drive 1.

The following message infact appears on the display:

0 = No printer connected

1 = Serial printer

2 = Parallel printer

The operator then depresses key "0" or key "1" or "2" depending on the error logging desired.

To exit to main menu the operator depresses the key "q".

The operator then has to answer a series of questions regarding the particular configuration of the system in use, as shown below.

Drive(s) to test: 0 = Drive 0 (default)
 1 = Drive 1
 2 = Both 0 and 1

Enter Selection:

Single Sided Drive? 1 = Yes (160KB)

Enter Selection:

Number of Tracks 0 = 35 Tracks (160/320KB)
 1 = 40 Tracks (160/320KB)
 2 = 70 Tracks (640KB)
 3 = 80 Tracks

Enter Selection:

Reformat Diskette(s)? 0 = No (default)
 1 = Yes

Enter Selection:

Compare Memory data? 0 = yes (default)
 1 = no

Enter selection:

Enter number of expansion board(s) (0 to 3)?

A menu of all the possible tests is then displayed. The following is the menu that appears on the Display after the operator has chosen the error logging option:

- 1 Video Alignment Test
- 2 Z8001 test
- 3 LSI Chip Test
- 4 Keyboard Test
- 5 Memory Test
- 6 Mini-Floppy Disk Test
- 7 RS 232C Interface Test
- 8 Parallel Interface Test
- 9 Parallel Printer Test
- 10 Mini-Floppy Disk Write Protect Test
- 11 Mini-Floppy Alignment and Eccentricity Test
- 12 Auto Test (tests 2-8)
- 13 System Exercisor

- 14 Operator Entered Test List
- 15 Configure System Test

The operator can depress CONTROL (BLUE SHIFT) and "C" keys simultaneously to interrupt any of the above tests and return to the main menu.

6.3 TEST DESCRIPTION

The following is a description of the various tests.

6.3.1 VIDEO MODULE TEST (SELECTED BY DEPRESSING '1')

The purpose of this test is to verify the correct operation of the video controller circuit and the display unit. Various video test patterns are displayed. These are arranged in such a manner that proper alignment of the CRT display can be checked. The video test menu is as follows:

- 0 = Graphics Pattern Test (default)
- 1 = Character Pattern Test
- 2 = Reverse Video Character Test
- 3 = Screen Illumination Test
- 4 = Colour Bars Test
- 5 = Full Screen Coloured Test
- 6 = Exit from Video Alignment Test

For each test the operator can depress any key to obtain the test pattern displayed on the screen. Also, the operator can depress any key to return to video test menu. To return to main menu the operator depresses the key "6". The operator may select any series of colour bars up to the limit of the system to display at one time. That is the operator may select four different colours for the four colour system and eight for the eight colour system. No restrictions are placed on the operator selection. However, should the operator enter a larger number than seven, the program only looks at the least three significant bits.

6.3.2 CPU TEST (selected by depressing '2')

All registers (excluding the refresh counter) are checked to verify that all bits can be set to zero and one. The following addressing modes are tested on the Z8001 CPU chip: register, Immediate, Indirect register, Direct Address, Indexed Address, Relative Address, Base Address, and Base Indexed Address.

The following instruction classes are tested on the Z8001 CPU: Load and Exchange, Arithmetic, Logical, Control, Bit manipulation, Rotate and shift, Block transfer, Input and output.

The following modes are tested: system, normal, segmented, and non-

segmented.

The following traps are tested: vectored interrupt, non-vectored interrupt, system call, privileged instruction.

The operator has the option of choosing whether he wants the CPU test to run in LOOP MODE or NO. To exit from loop mode the operator has to depress the CONTROL (BLUE SHIFT) and "C" keys simultaneously.

6.3.3 LSI CHIP TEST (SELECTED BY DEPRESSING '3')

This test tests the functionality of the following integrated circuits: both 8251 USARTs, 8253 Timer, 8255 Parallel I/O chip, 6845 CRT Controller, 1797 floppy Disk controller. Various registers are tested as well as the chip enable logic and the data paths to the chips.

The operator has the option of choosing whether he wants the LSI test to run in loop mode or not. To exit from loop mode the operator depresses the CONTROL (BLUE SHIFT) and "C" keys simultaneously.

6.3.4 KEYBOARD TEST (SELECTED BY DEPRESSING '4')

The purpose of this test is to determine if all of the mechanical switches, electronics, and the bell functions are working properly. The keyboard self test and bell function are first tested ten times. The keyboard country is then displayed on the CRT Display for verification by the operator. The keyboard layout then appears on the screen and the operator is asked to depress the key indicated by the cursor. There are four modes of operation: Unshift Mode, shift Mode, Control Mode, Command Mode. To advance from one mode to the next the operator has to depress 'S2' key. To exit from the test, the operator has to depress 'S2' key while in COMMAND mode.

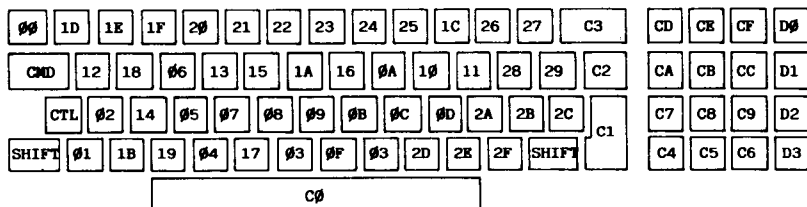


Fig. 6-1 M20 Keyboard with UNSHIFT MODE Raw Keycodes

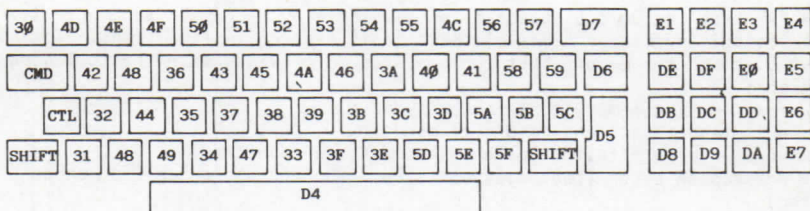


Fig. 6-2 M20 Keyboard with SHIFT MODE Raw Keycodes

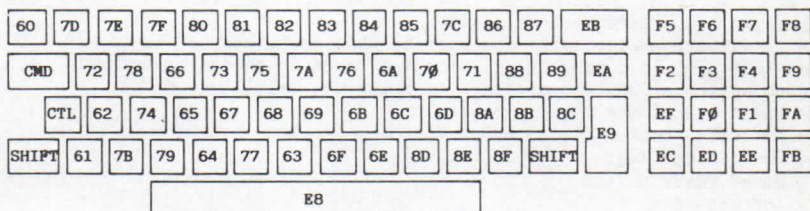


Fig. 6-3 M20 Keyboard with CONTROL MODE Raw Keycodes

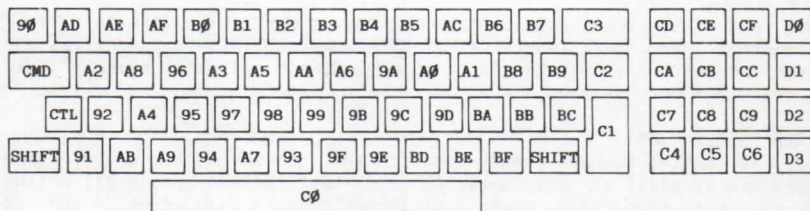


Fig. 6-4 M20 Keyboard with COMMAND MODE Raw Keycodes

6.3.5 MEMORY TEST (SELECTED BY DEPRESSING '5')

The RAM test includes 5 separate tests which are executed sequentially. The default number of times of these tests are run is five times. After having chosen the memory test the operator is provided with the following options:

- 0 = test (entire memory test is carried out)
- 1 = quit (abort test and return to menu)
- 3 = stop on error (test stops on first error encountered)
- 5 = no stop on error (test does not stop, even if an error is encountered)
- 2 = display banks (memory banks are displayed)
- 4 = print banks (memory banks are printed)
- 6 = test bank(s)

The operator depresses any of the above keys. For example, the operator depresses the key "3", followed by carriage return, followed by "0", followed by carriage return, if he wants to run the memory test and stop on error.

The operator then has to select the options for the test. By inserting only a carriage return for the selection, the default value (as displayed) is entered automatically.

The first option allows the operator to choose whether he wants to run the test in loop mode or no. The loop mode is chosen by default. The second option allows the operator to enter the testing sequence.

The memory tests are the following:

- 0 = Default Sequence (1,2,3,4,5,6,7)
- 1 = Bank Select Test
- 2 = Fixed Pattern Test
- 3 = Address Test
- 4 = Marching Test
- 5 = Buss Noise Test
- ' = Moving Inversion Test
- = Refresh Test

To exit from the memory test and return to main menu the operator has to depress 'CONTROL' and 'C' keys simultaneously.

The following is a description of each of the 7 tests that are performed:

BANK SELECT TEST

This test writes into each 16K bank its bank number. The test then verifies that each bank contains its bank number. This test verifies the correct operation of the bipolar mapping ROM, and all chip select logic to the RAM memory devices.

FIXED PATTERN TEST

This test writes to each memory location the current test pattern and immediately verifies the pattern. The test cycles through all of the memory twenty four times, using a different pattern each time. The 24 patterns in hexadecimal format are:FFFF, 0000, 5555, 0101, 0202, 0808, 1010, 2020, 4040, 8080, FEFE, FDFD, FBFB, F7F7, EFEF, DFDF, 8F8F, 7F7F, FF00, 00FF, AA55, 55AA.

ADDRESS TEST

This test writes into each memory location its address. The memory is then checked to verify the addresses. This test is done by using byte operations so that it can first be done using even addresses and then

using odd addresses. The test is then repeated writing the complement of the address into memory location. Thus all of memory is written and read four times in this test.

MARCHING TEST

The same twenty four fixed patterns used in the fixed pattern test are used in this test. The memory is first filled with the first pattern. Starting at the beginning of memory the pattern is read and verified, and then the complement of the pattern is written into the cell and verified. The test then goes to the next cell and repeats the same process until the end of memory is reached. When the end of memory is reached the test starts backwards verifying the pattern, complementing it, storing it, and verifying it. This is repeated for each cell until the beginning location is reached. This process is repeated for all 24 patterns. All of memory is written and read 96 times in this test.

BUSS NOISE TEST

This test uses two unique instructions of the Z8001 CPU to exercise the memory, address and data busses. The test fills the memory with a pattern using the LDIR (Load, Increment and Repeat) instruction. Memory is then checked using the CPIR (Compare, Increment and Repeat) instruction. This is repeated using all 24 fixed patterns. This entire sequence is then repeated 8 times. All of memory is written and read 192 times.

MOVING INVERSION TEST

This test is useful in uncovering pattern sensitivity in the RAM devices. The test uses a complex algorithm in which a field of zero bits is inverted and then reinverted again with each pass. This process is repeated using address steps which with each pass are multiplied by two. The test is run first with a forward sequence and then a backward sequence. Several main characteristics of this algorithm are that each write is between two read actions, and that addresses are generated in different increments and directions.

REFRESH TEST

This test first writes a zero pattern to all banks under test. The test then delays 10 seconds and verifies that all memory locations still contain the zero pattern. This is repeated using an FFFF pattern. This test verifies that the RAM memory is being correctly refreshed by the video display circuitry.

6.3.6 MINI-FLOPPY FUNCTIONAL TEST (selected by depressing '6')

The program instructs the operator to insert a scratch diskette into the drive under test. A diskette must be used on which the entire surface will be written.

The operator then selects the options for the test. By depressing only a carriage return for the selection, the default value (as displayed) is entered automatically.

The operator is asked if he wants to run the test he chooses in loop mode or not.

The operator then chooses the tests he wants to carry out sequence.

The tests available are:

0 = Default sequence (1,4,5,2,3,5)
1 = Write Tracks 1 to Max
2 = Write Tracks Max to 1
3 = Read Tracks 1 to Max
4 = Read Tracks Max to 1
5 = read Random tracks
6 = Read Track Max

To exit from the mini-floppy disk test the operator has to depress the

TEST 1 : Test 1 writes the current test patterns to the diskette starting with track 1 and continuing to track 34. Following each track write a verify operation is performed. The verify operation reads the entire track but does not do a data comparison on the data read. Side zero is written and verified first and then side one is written and verified.

TEST 2: Test 2 writes the current test patterns to the diskette starting with track 34 and continuing to track 1. Following each track write a verify operation is performed. The verify operation reads the entire track but does not do a data comparison on the data read. Side zero is written and verified first and then side one is written and verified.

TEST 3: Test 3 reads the diskette starting with track 1 and continuing to track 34. Following each track a verify of the data read is performed if this option is turned on. Side zero is read and verified first and then side one is read and verified.

TEST 4: Test 4 reads the diskette starting with track 34 and continuing to track 1. Following each track a verify of the data read is performed if this option is turned on. Side zero is read and verified first and then side one is read and verified.

TEST 5: Test 5 reads a random track and verifies the data if that option is turned on. Side zero is read and verified first and then side one is read and verified.

TEST 6: Test 6 reads track 34 and verifies the data. Side zero is read and verified first and then side one is read and verified.

TEST PATTERNS

Each sector is written as follows: the first byte is the track number, the second byte is the side number, and the third byte is the sector number. The remaining 253 bytes contain one of the five different test patterns. In the first four patterns all of the 253 bytes are the same. The byte patterns (in hexadecimal) are: E5, B6, 99, and A1. The fifth pattern is an incrementing pattern: byte 4 contains a 3, up to byte 256 which contains an FF (hex).

The patterns are written with pattern 1 in sector 1, pattern 2 in sector 2 up to pattern 5 in sector 5, and then starting over with pattern 1 in sector 6. On each pass of the test the patterns written to each sector are changed by one, so that after 5 passes each sector on the diskette contains all 5 patterns. (During the second pass pattern 2 is written to sector 1, pattern 3 to sector 2, etc. During the third pass pattern 3 is written to sector 1, pattern 4 to sector 2 etc.)

TESTING DISPLAYS

A status indicating the current test, the drive number, track number, and

side number are continually displayed on the display during the test. Following each complete pass of the test sequence the pass and error count are displayed on the display.

6.3.7 RS 232C INTERFACE TEST (SELECTED BY DEPRESSING '7')

This test requires a jumper to be connected to the RS 232C serial port on the motherboard. This jumper connects the following signals: RxD to TxD, RTS to CTS, and DSR to DTR. The jumper pin configuration is given at the end of this chapter. The STAC code for this jumper is 578451 Y. Check also that the TNSPR jumper block on motherboard is configured as follows:

T to T2;
N2 to P2;
P to P1;
S to S2;
R to R1;

The test program verifies the correct operation of the handshake lines by placing data patterns on the DTR output line, and then reading the DSR status bit. This verifies the DSR and DTR functions within the USART and the buffers. The RTS is then made inactive and an attempt is made to send and receive data. If the RTS output and the CTS inputs are working properly, no data should be received. The RTS is made active and the attempt is made again. This time the data should be received. This verifies correct operation of the RTS and CTS functions of the USART and line buffer and receiver.

The TxD and RxD and associated buffer and receiver are tested by sending out streams of various data and checking to make sure they are received. This section is interrupt driven and tests the RxRDY and TxRDY lines from the USART (which are used to generate the interrupts). Provisions are also made to allow looping on the USART programming, the handshake tests and the transmit-receive test. This allows easy debug of problems on the RS 232C interface.

To exit while in loop mode the operator depresses 'CONTROL' and 'C' keys simultaneously.

6.3.8 PARALLEL INTERFACE TEST (SELECTED BY DEPRESSING '8')

This test requires a jumper to be connected to the parallel port on the motherboard. The jumper connects the A port (outputs) to the B port (inputs), and connects the various handshake signals used on Port C. The STAC code for this jumper is 5784854V.

This test writes all 256 binary patterns to the output port and reads the input port after each output to verify the correct operation. The handshake signals are implicitly tested.

This test allows looping on programming of the 8255, and looping on either of the port tests.

6.3.9 PARALLEL PRINTER TEST (SELECTED BY DEPRESSING '9')

The printer tests prints a standard message to the parallel printer port so that the operator can visually verify the correct operation of the printer attached to the M20 system.

6.3.10 MINI-FLOPPY WRITE PROTECT TEST (SELECTED BY DEPRESSING '10')

The floppy disk write protect test provides the operator with the option of performing the test on drive 0 (default drive) or on drive 1 or on both drives.

The operator is then asked if he wants to perform this test in a loop mode or not. The default is YES.

The operator is then asked if he wants to perform this test in a loop mode or not. The default is YES.

The operator is then asked to mount a write protected diskette into the disk drive(s) he has chosen to test. The operator can then press any key to begin the test and the write protect function of the drive in question is tested.

On the CRT Display the operator is informed whether this test has been successful or not.

6.3.11 MINI-FLOPPY ALIGNMENT & ECCENTRICITY TEST (SELECTED BY DEPRESSING '11')

This test requires the use of the MARGINED DISK (STAC code 000477G). The operator is then asked to insert the margined disk into the drive under test. Upon completion of the test the operator is instructed to reinsert the system test diskette.

The margined disk allows the software to check the alignment and performance parameters of the floppy disk drive. This test is a read only test, so that the contents of the diskette are not destroyed. This test consists of reading specific patterns in specific locations on the diskette.

6.3.12 AUTO TEST (SELECTED BY DEPRESSING '12')

This test performs tests 2 to 8 already described: CPU test, LSI chip test, keyboard test, memory test, mini-floppy disk test, RS 232C interface test and parallel interface test. The auto test loops continually and the operator has to depress 'CONTROL' and 'C' simultaneously to return to main menu. At one point in this test the CRT display appears dark for a couple of seconds. This occurs during the memory test when the memory area is being filled up with zeroes.

6.3.13 SYSTEM EXERCISOR TEST (SELECTED BY DEPRESSING '13')

The purpose of this test is to check the system for any interactive faults. The system exercisor simultaneously tests many functions. The following are intermixed in a random fashion: Serial port transmit and receive interrupt processing, floppy disk I/O, parallel port processing, memory and video tests.

6.3.14 OPERATOR ENTERED TEST LIST (SELECTED BY DEPRESSING '14')

This test allows the operator to choose a particular sequence of tests he desires.

In fact after the question "Loop Mode or No?" the message:

ENTER ANY SEQUENCE OF TESTS

appears on the screen.

Note: Insert the number of each test desired separated by a space.

6.3.15 CONFIGURE SYSTEM TEST (SELECTED BY DEPRESSING '15')

This test configures the particular system under test. In fact it is a repetition of the questions that appear before the main system test menu appears.

6.4 ERROR MESSAGES

The following section describes the types of messages from the various tests.

6.4.1 VIDEO MODULE TEST

Since this test relies entirely on the operator to determine if the display is correct and the CRT is aligned properly, no errors that the computer can recognize are possible in this test.

6.4.2 Z8001 CPU TEST

Message displayed: Z8001 CPU TEST FAILED

6.4.3 LSI CHIP TEST

Message displayed: LSI CHIP TEST FAILED

The specific name of the faulty LSI chip is also displayed. The LSI chips are the following:

8251 (Keyboard Interface)
8251 (Serial Interface)
8253 (Timer)
8255 (Parallel Interface)
6845 (CRT Controller)
1797 (Floppy Disk Controller)

6.4.4 KEYBOARD TEST

Message displayed at bottom of screen:

ERROR Raw Keycode is XX Should be YY
where XX = incorrect code of key depressed
and YY = correct code of key depressed

Errors are displayed immediately on occurrence. All the key codes are shown in figures 5-1 to 5-4.

6.4.5 RAM MODULE TEST

Any error occurring during the test is displayed on the CRT. The message contains the test number that failed, the address of the failure, a binary printout of what the data should look like, and what the data read actually looked like.

As each of the five tests is executing the test number is displayed on the CRT. Following each cycle through the entire test sequence the pass number and total error count is displayed on the CRT screen.

RAM ERRORS

The following RAM memory addresses are physically located on the motherboard: Bank 00 Range: (00)0000 to (00)3FFF

Bank 01 Range: (01)8000 to (01)BFFF

Bank 02 Range: (03)0000 to (03)3FFF

Bank 03 Range: (05)0000 to (05)3FFF

Bank 04 Range: (05)4000 to (05)7FFF

Bank 05 Range: (05)8000 to (05)BFFF

Figure between parenthesis denotes the segment number.

Following table attempts to identify the faulty RAM chip on the motherboard:

FAULTY DATA BIT

FAULTY RAM CHIP

D0	U105
D1	U104
D2	U103
D3	U102
D4	U101
D5	U100
D6	U99
D7	U98
D8	U115
D9	U116
D10	U117
D11	U118
D12	U119
D13	U120
D14	U121
D15	U122

The following memory addresses are physically located on the first memory expansion board (B/W):

range (01)C000 to (01)FFFF

range (0A)8000 to (0A)BFFF

The following memory addresses are physically located on the second memory expansion board (B/W):

range (08)8000 to (08)BFFF

range (0A)C000 to (0A)FFFF

The following memory addresses are physically located on the third memory expansion board (B/W):

range (08)4000 to (08)7FFF

range (03)8000 to (03)BFFF

The following table attempts to identify the faulty RAM chip on a B/W memory expansion board:

FAULTY DATA BIT

FAULTY RAM CHIP

D0	U2
D1	U3
D2	U4
D3	U5
D4	U6
D5	U7
D6	U8
D7	U9
D8	U11
D9	U12
D10	U13
D11	U14
D12	U15
D13	U16
D14	U17
D15	U18

The following table attempts to identify the faulty RAM chip on a colour memory expansion board:

FAULTY DATA BIT	FAULTY RAM CHIP
D0	U8
D1	U7
D2	U6
D3	U5
D4	U4
D5	U3
D6	U2
D7	U1
D8	U9
D9	U10
D10	U11
D11	U12
D12	U13
D13	U14
D14	U15
D15	U16

EXAMPLE:

Error in test -

Address (01)C000

Value is 00000000 00000001

Should be 00000000 00000000

This means that error occurred at address (01)C000 i.e. on First Memory Expansion Board.

Faulty bit is D0 i.e. chip U2 is most probably the faulty component.

6.4.6 MINI-FLOPPY DISK TEST

Write Errors: If an error occurs while writing a track, the error is displayed and one attempt is made to write the track again. If an error is encountered during the verify operation, the error is displayed, and one retry is made on the verify operation. If an error occurs on the second verify, the error is displayed and the write and verify operation are attempted one more time.

Read Errors: If an error occurs while reading a track, the error is displayed and one attempt is made to read the track again. If an error occurs during the data comparison, the read and comparison operation are attempted one more time.

ERROR PRINTING FORMAT:

When an error occurs, the type of error is displayed along with the test number, drive number, track number and side number. The mini-floppy disk controller chip status register is then examined and the various types of errors are printed also. The following possible errors are displayed from the status register: Drive not ready error, write protect error, write fault error, record not found error, CRC error, and lost data error.

Drive Not Ready Error	No diskette present in disk drive
Write Protect error	Write protect notch covered
Write Fault error	Fault occurred on write operation
Record not found error	Desired sector, track or side were not found
CRC error	Cyclic Redundancy Check error. *
Lost Data error	The M20 did not respond to the DRQ(Data request) in one byte time.

*CRC is a check carried out to detect errors. For further details on CRC refer to mini-floppy disk interface section.

6.4.7 RS 232C INTERFACE TEST

The type of error occurring is displayed and the user has the option of entering several looping states.

Example of error message:

***ERROR DTR to DSR not correct

6.4.8 PARALLEL INTERFACE TEST

The type of error occurring is displayed, and the operator has the option of entering several looping states for diagnostic purposes.

Example of error message:

***ERROR Port A to Port B Test

Data was 3F

Data should be 00

6.4.9 WRITE PROTECT TEST

The operator is informed on the CRT Display whether the write protect has been detected or not.

6.4.10 FLOPPY DISK ALIGNMENT TEST

This test displays the type of alignment failure. Failures in this test must be corrected before the floppy disk functional test (6) can be performed.

Figure 6-5 shows the errors displayed on the CRT screen. The internal tracks are those numbered 16-30 and the external tracks 2-16.

The first section of figure 6-5 gives information regarding the nature of the error (distributed or consecutive) as well as whether they were internal or external and the track they occurred on. It also informs the operator on what side of the disk and on what drive the test was carried out.

The second part displays the number of tracks read and the errors found during the read operation. Anything but '00' indicates an error has occurred on the track.

The third part gives the alignment and eccentricity values of the drive under test as well as indicating the number of tracks that had no errors.

NOTE: Values recommended for correct operation of the drive are:
Alignment = 60 microns
Eccentricity = 60 microns

At the end of the test the user has to verify that the sum of the eccentricity and alignment values does not exceed 110 microns.

If the sum is greater than 110 microns, the disk drive must be adjusted with the alignment disk.

1) <u>FIRST TRACK FOUND WITH:</u>	<u>INTERNAL</u>	<u>EXTERNAL</u>	(DECIMAL NUMBERS)
2 Distributed Errors or more:	XX	XX	DRIVE = 0 or 1
8 Distributed Errors or more:	XX	XX	
8 Distributed Errors or more:	XX	XX	SIDE = 0 or 1
All 16 Sectors have Errors :	XX	XX	

2) <u>TRACK NUMBER</u>	:	<u>16</u>	<u>17</u>	<u>18</u>	<u>19</u>	<u>20</u>	<u>21</u>	<u>22</u>	<u>23</u>	<u>24</u>	<u>25</u>	<u>26</u>	<u>27</u>	<u>28</u>	<u>29</u>	<u>30</u>
Distributed Errors:		ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ
Consecutive Errors:		ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ

2) <u>TRACK NUMBER</u>	:	<u>16</u>	<u>15</u>	<u>14</u>	<u>13</u>	<u>12</u>	<u>11</u>	<u>10</u>	<u>09</u>	<u>08</u>	<u>07</u>	<u>06</u>	<u>05</u>	<u>04</u>	<u>03</u>	<u>02</u>
Distributed Errors:		ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ
Consecutive Errors:		ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ	ZZ

3) <u>ALIGNMENT</u>	=	NN Microns (Internal / External)	<u>ECCENTRICITY</u>	=	NN Microns
<u>PASSING</u>	:	Number of tracks with 9 good sectors	=	NN (Min. 15)	

N.B. - NN = Decimal Value
XX = Track Number
ZZ = Number of Sectors Errors

Fig. 6-5 Table displayed after the end of the Floppy Disk Alignment Test

6.4.11 SYSTEM EXERCISOR TEST

In addition to the type of error which occurred, the error message also describes the environment in which the failure occurred, so that interactive faults can be detected easily. although the sequence of tests is based on a random number generator, the same sequence can be repeated by using the same random number seed.

6.4.12 JUMPERS REQUIRED FOR SYSTEM TEST

The following jumpers and configurations are required for the I/O port tests:

Parallel Loopback Jumper Connector (Code: 5784854 V)

NAME	Pin	to	Pin	Name
PA0	4	to	32	PB0
PA1	6	to	22	PB1
PA2	8	to	30	PB2
PA3	10	to	24	PB3
PA4	12	to	26	PB4
PA5	14	to	28	PB5
PA6	16	to	34	PB6
PA7	18	to	36	PB7
PC5	2	to	20	PC6

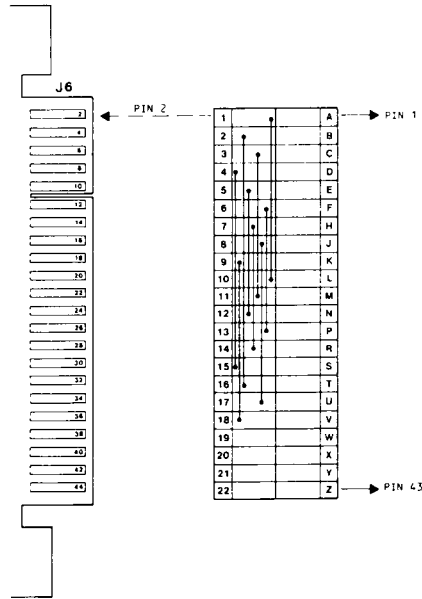


Fig. 6-6 Parallel Loopback Jumper Connector

Serial Loopback Connector (Code: 5784851 Y)

Name	Pin	to	Pin	Name
TXD	2	to	1	RXD
CTS	6	to	5	RTS
DTR	4	to	3	DSR
DTR	4	to	10	Ring Detect
DTR	4	to	12	Signal Detect

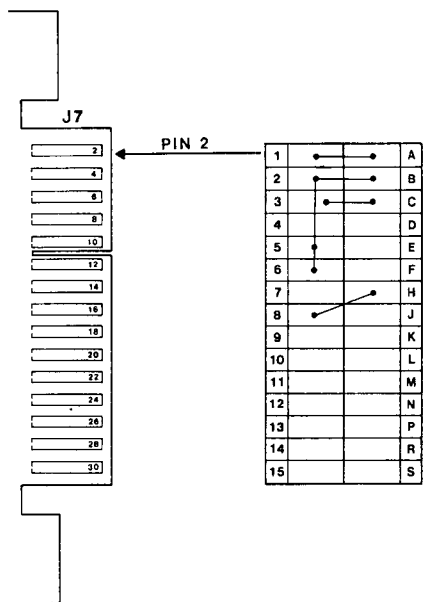


Fig. 6-7 Serial Loopback Connector

The following jumpers must be present for the serial port test: T to T2

N2 to P

P to P1

S to S2

R to R1

Code of margined disk: 000477G

6.5 SYSTEM TEST FOR HARD DISK

The system test for the Hard Disk Unit is resident on a separate mini-floppy disk. The disk is used by field engineers for the Hard Disk functional test. This disk is independent of the other system test disk described previously. This test is carried out by the same hardware drivers of the PCOS operating system. Besides the test programs, information is given to find faults on the Hard Disk.

6.5.1 OPERATING PROCEDURES

The Hard Disk System Test Disk is loaded from the mini-floppy disk drive at the end of the power-up diagnostics. The error logging option is then displayed. The operator can select among the following:

- errors displayed on video only
- errors displayed on video and printed by serial printer
- errors displayed on video and printed by parallel printer
- errors displayed on video and error logging on mini-floppy disk

For the above choice the following message is displayed:

0 = no printer connected

1 = serial printer

2 = parallel printer

3 = log errors to disk (the user is requested to give the system and operator identification number. This option is only used by Production).

The operator hits keys 0,1,2,3 according to the desired error logging.

A menu of all the available tests is then displayed.

1. drive ready test
2. seek test
3. data pattern test
4. random write, read and verify
5. insert test
6. funnel test
7. scantion test
8. ageing test
9. controller test
 - a. full exercise
 - b. write/continous verify
 - c. format
 - d. set parameters
 - e. HDU debugging options
 - f. scope loop selection

The above tests can be interrupted by hitting the numeric key "1". It is useful for the operator to bear in mind the following information on the Hard Disk when performing the above tests:

6 Read/Write Heads
3 Platters
6 Surfaces
1080 Tracks
33 Sectors/Track
180 Cylinders

6.5.2 DRIVE READY TEST (SELECTED BY DEPRESSING '1')

The drive ready test assures that the hard disk drive is ready. If the drive is not ready in 15 to 17 seconds an error message is displayed.

6.5.3 SEEK TEST (SELECTED BY DEPRESSING '2')

On selecting this test the following message is displayed:

"Is bad block list on disk? (1=yes)"

If the operator depresses the numeric key '1' the test automatically starts. If the operator depresses any other character or number besides '1' he is asked to input the cylinder numbers, head numbers, and sector numbers.

The first seek is to cylinder 179, the second to cylinder 0, the third to cylinder 178, the fourth to cylinder 1 and so on. Any error indicated in the status register causes the program to increment a counter. Operator honoured parameters are honoured, but at least two cylinders must be entered (i.e. start cylinder = 0 last cylinder = 1 as a minimum). The test loops until the operator depresses '1' at the keyboard.

6.5.4 DATA PATTERN TEST (SELECTED BY DEPRESSING '3')

The pattern test writes all cylinders with a data pattern, and then verifies that pattern. The disk is written from the lowest specified cylinder to the last cylinder specified. A read and verify in memory is then performed in a similar way. This sequence is then repeated from the last cylinder to the first. The write starts with the cylinder specified in the memory location st-cyl (initialized to 0), head specified at memory location st-head (initialized to 0), and sector specified at memory location st-sec (also initialized to 0). The write increments from these initial values up to and including the values specified in memory locations last-cyl, last-head, and last-sec. (these are initialized to 179, 5 and 31 respectively)

This allows the operator to test a specific area of the hard disk. The verify starts with the last values specified by memory locations last-cyl, last-head, and last-sec. Therefore the first sector written is the last read and verified. This provides a partial aging test. The data pattern is the suggested worst case for the drive. This pattern is used as a default, and can be altered with the set parameter function.

Operation time outs are reported as an error, the time allowed is sufficient for all retries to take place. The remaining errors are divided into HARD and SOFT errors.

HARD ERRORS: Hard Errors are generated by the error bit in the status register. Reported are the cylinder, head, sector, and the contents of the error register. These errors are defined as follows:

bit 0.....DAM (Data Address Mark) not found
bit 1.....TRO (track 0) error
bit 2.....aborted command
bit 3.....undefined
bit 4.....ID (identification) not found
bit 5.....CRC (Cyclic Redundancy Check) error - ID field
bit 6.....CRC (Cyclic Redundancy Check) error - data field
bit 7.....Bad Block Detect

SOFT ERRORS: Soft errors are a result of a good transfer from the hard disk controller, but the data received was not identical to the data written to the disk. The following data pattern is repeated for 256 bytes:

DB 6D DB 6D B6 DD B6 DD 6D DB 6D DB DD B6 DD B6

This pattern is generated by using two word values. Word one is written twice, then word two is written twice, the high and low bytes of these words are exchanged, and the sequence is then repeated. These initial values may be altered by the operator. For example the initial values of AA55 and FF00 would produce the same repeated pattern in the buffer:

AA 55 AA 55 FF 00 FF 00 55 AA 55 AA 00 FF 00 FF

This pattern is written to a buffer in memory for 256 bytes, and then the cylinder address, head number, and sector number are written consecutively over the first three bytes. This test runs until the operator enters a '1' at the keyboard.

6.5.5 RANDOM WRITE, READ AND VERIFY (SELECTED BY DEPRESSING '4')

Random write, read and verify saves the current start and last values. The cylinder, head, and sector values are taken from a random number generator. These values are then put in the start and last values. The data pattern test is then called. This does the write verify to only one discrete sector. This operation is repeated 100 times. The initial start and last values are restored, the information displayed, and a check is made for operator termination request. When invoked individually, the cylinder head, and sector information is presented at the completion of the write, read and verify. However, when invoked in the full exerciser, only the cylinder number is presented.

NOTE: The user entered parameters are not honoured as the start and last values (the data pattern is altered, but that is the only value entered by the operator that this test honours).

6.5.6 INSERT TEST (SELECTED BY DEPRESSING '5')

The insert test uses some of the routines available in the data pattern test. The entire disk is written and verified with the data pattern specified by the operator (or default). The test then writes and verifies all odd sectors on even cylinders and even sectors on odd cylinders with complemented data pattern (as always the cylinder/sector/head value are in the first three bytes). Finally the test reads and verifies all the entire disk (the parameters are honoured by the test; however, sectors should always start on an even sector number and at least 2 sectors should be tested or else the test incorrectly reports errors).

6.5.7 FUNNEL TEST (SELECTED BY DEPRESSING '6')

The funnel test writes an incrementing pattern (first three bytes are as usual the cylinder, head and sector) to the disk. The pattern of the write, read, and verify is however different. Each individual cylinder/surface is written one sector at a time. The sectors are written in the following manner: start sector, last sector, start sector + 1, last sector - 1, and so on down to the centre sector. The surface pointer is then incremented and the process repeated until all the surfaces have been tested. This process is then repeated until all cylinders have been tested in this manner. Test runs until the operator enters a '1' at the keyboard.

6.5.8 SCANTION TEST (SELECTED BY DEPRESSING '7')

The scantion test writes and verifies the entire disk. A random number is then generated and used as a key. All sector numbers are equal to the key on all surfaces and cylinders are written to and verified. This operation is then repeated for all sector numbers less than the key. Finally, the write and verify is then performed on the sector numbers greater than the key.

6.5.9 AGEING TEST (SELECTED BY DEPRESSING '8')

The ageing test is a very long test. The sectors are written and verified individually. Then all sectors previously written are then read and verified. The ageing test loops until the operator enters '1' at the keyboard. NOTE: With the default parameters the cylinder display may appear confusing. EXAMPLE: Test is currently writing cylinder 5, head 3, sector 1E. After the write of the selected sector all heads and sectors from cylinder 4 to cylinder 0 are read and verified. Then all sectors are read and verified from heads 2 to 0. Then all the sectors up to and including 1E are read and verified. Sector 1F is then written and verified and the read verify process is repeated until all of the disk

specified has been tested.

6.5.10 CONTROLLER TEST (SELECTED BY DEPRESSING '9')

The controller test writes, reads and verifies all possible data to the ports that allow both writes and reads. Proper operation of the busy bit, and proper status when not busyb are then verified. The remainder of the test is performed only if a bad block is mapped. A read is attempted of the bad block and proper operation of the error bit and the error register are then verified.

6.5.11 FULL EXERCISE (SELECTED BY DEPRESSING 'A')

The full exercise repeatedly performs tests 1 through 6 until the operator enters the character '1'. At the end of each pass the counter information is presented to the operator. Pass number, total error count, and an error count breakdown are all presented to the operator. If the operator elects to stop in the middle of the test, the current pass is completed before the task is terminated. The pass number is not incremented until the current pass is completed. The information display is presented at the end of all the individual tests, and during the first pass the counter displays 0.

6.5.12 WRITE/CONTINUOUS VERIFY (SELECTED BY DEPRESSING 'B')

Write/Continuous verify test writes once as per the data pattern test and then performs the read/verify function of the data pattern test repeatedly. Information presented and task termination are the same as the above tests. The set parameter command allows the operator to perform a "read only". No write takes place at the start of the test. This test should be used with great caution. Therefore it is advisable to select the read only option after a full write test is performed on the unit. The operator should remember that the read only option expects the current data pattern seed to be used to write to the disk.

6.5.13 FORMAT (SELECTED BY DEPRESSING 'C')

Format starts by prompting the operator for the bad block physical sector number. Please note this routine sets up for a 4 to 1 interleave, and so the physical sector number is not the same as the logical sector number to the software. Errors are all reported in logical sector numbers. To enter the last value a carriage return in response to each of the three queries from the M20 terminate the bad block entry. Bad sectors are marked in the format as bad blocks. This results in an error status of

80 hexadecimal. In the error routines if this error occurs, and there is one bad sector on that cylinder no error is reported.' Thus the known bad characters are hidden from the user. The disk is then formatted by the controller. The user entered parameters are honoured by the format routine and hence it is possible to format only a few cylinders. Please note that the operator need only enter the bad block information once during a session. Further requests for formatting do not prompt for bad block information. At the end of the procedure the entire disk is verified to see if it contains all the specified data (all 0s in the data fields).

6.5.14 SET PARAMETERS (SELECTED BY DEPRESSING 'D')

Parameters may be set for the tests with the exception of the random test. The operator is allowed to change the seek pattern of tests two, first pass of four, six and seven. Those presented are the alternatives to the default. The default pattern is write from cylinder 0 to 179, and then read/verify from cylinder 179 to 0. First the operator is given the opportunity to select the funnel test pattern. This pattern is for both write and read/verify. The pattern is start cylinder, last cylinder, start +1, last -1, and so on. Selection of the funnel test pattern overrides any other seek pattern for these tests. The operator enters '1' to select the pattern. Should the operator not desire the funnel test pattern he has the option of choosing the direction for the write and read/verify pattern ('1' entered selects the optional pattern). This selection is offered only if the funnel test pattern is not selected. The operator is asked for the start values and then the last values. The operator

is then given the option of entering the two data words used to generate the data pattern used in all the tests (except the seek test and the adjustment tasks). A '1' enables this change and any other key terminates the task. The write with continuous verify can be made into a NOTE: The same patternseed words that were used to write the entire disk must be present.

6.5.15 HDU DEBUGGING OPTIONS (SELECTED BY DEPRESSING 'E')

A series of options are selected from a menu presented to the operator. The operator is prompted for and must enter the desired cylinder, head and sector. A write or read command is then issued to the controller. The keyboard status is tested, if an input is pending the task is terminated. When no input is pending from the keyboard, the task waits for the controller busy bit to become false. The sequence is then repeated. The write has been modified to prompt for two data words. These words are then used to fill the write buffer. The write adjustment writes the data specified out to the disk.

In addition to the read and write adjustment, the remaining commands are also available in a loop mode. A format loop formats the selected cylinder until the operator strikes any key. Also the seek test performs continuous seeks to the selected cylinder, head, and sector. The restore

loop continues to issue a restore command to the controller until the operator strikes a key. Newly available are two display options. The user may select to view the bad block list or the specific sector hard error counter. The operator must enter the desired head number to view that collection of counters. The bad block list only displays a fixed number of entries at a time. The operator is then required to strike any key to continue the listing.

6.5.16 SCOPE LOOP SELECTION (SELECTED BY DEPRESSING 'F')

A menu of all the scope loops available is displayed. The operator then responds to the prompts for the port address (es) and data as required by the loop. The write read loop writes the data entered to the first port selected, and then writes the second data to the second port selected. The read loop continuously reads the port selected. The address loop alternatively reads the two ports selected. Any key entered terminates the loop.

6.6 SYSTEM TEST FOR TWIN RS 232C BOARD

The system test for the Twin RS 232C Board is resident on a separate mini-floppy disk. This disk (code H0 5172) is used by field engineers to test the Twin RS 232C board and is independent of the other system test disks described previously. This test is carried out by the same hardware drivers of the PCOS operating system. Two types of loopback connectors described at the end of the section are needed for this test. All tests except test 2 need the RS 232C loopback connector. Test 2 needs the Current Loopback connector.

6.6.1 OPERATING PROCEDURES

The TWIN RS 232C Board system test is loaded from the mini-floppy disk drive at the end of the power up diagnostics. The error logging option is displayed. The operator can select among the following:

- errors displayed on video only
- errors displayed on video and printed by serial printer
- errors displayed on video and printed by parallel printer
- errors displayed on video and error logging on disk.

For the above choice the following message is displayed:

0 = no printer connected

1 = serial printer

2 = parallel printer

3 = log errors to disk (the user is requested to give the system and operator identification number. This option is only used by Production).

The operator hits keys 0,1,2,3 according to the desired error logging.

A menu of all the available tests is then displayed:

1. RS 232C Data Integrity
2. Current Loop Data Integrity
3. Control Lines
4. Synchronous Data Transfer
5. Baud Rate Accuracy
6. Interrupt Subsystem
7. Interrupt Driven Data Transfer
8. Default String (tests 1, 3-7)

If the operator chooses to run test 2, for example, he must depress the key '2' followed by carriage return.

6.6.2 TEST 1 RS 232C DATA INTEGRITY

Before proceeding with this test the operator must install the RS 232C loopback jumper to the connector (J35) at the back of the M20 Basic Module. See the end of this section for the loopback jumper configuration.

In this test all possible data is transmitted at the highest allowable baud rate (19.2 KBaud for asynchronous data transfers). The test is performed from serial port zero to serial port one, and then from serial port one to serial port zero. This allows the isolation of the faulty channel. Errors are reported for status, channel software time-out and data errors. If the test is successful the message "Test complete. Enter any key to continue test." appears.

6.6.3 TEST 2 CURRENT LOOP DATA INTEGRITY

Before proceeding with this test the operator must install the Current loopback jumper to the connector (J35) at the back of the M20 Basic Module. See the end of this chapter for the loopback jumper configuration.

In this test all tests are identical to those carried out in test 1 with the exception of the baud rate. If the test is successful the message : "Test complete. Enter any key to continue test." appears.

6.6.4 TEST 3 CONTROL LINES

Before proceeding with this test the operator must install the RS 232C loopback jumper to connector (J35) at the back of the M20 Basic Module. See the end of this chapter for the loopback jumper configuration. In this test the control lines of both serial channels are set and the proper reaction is tested at the other channel. The following lines are tested: RTS, CTS, DTR, DSR, Signal Detect, Ring Indicator, and the "break function".

The break function forces transmit data low for more than two character frames. Error messages are reported according to the serial port generating the control signals. If the test is successful the message "Test complete. Enter any key to continue." appears.

6.6.5 TEST 4 SYNCHRONOUS DATA TRANSFER

Before proceeding with this test the operator must install the RS 232C loopback jumper to connector (J35) at the back of the M20 Basic Module. See the end of this chapter for the loopback jumper configuration. The baud rate is initialized to 50 baud, and a synchronous data transfer of 64 bytes is performed. This transfer is performed by polling the serial port for transmitter ready, and for receiver ready. This transfer is performed in one direction only (from port 0 to port 1). Errors are reported for data integrity, and failure to synchronize. If this test is successful the message: "Test complete. Enter any key to continue". appears.

6.6.6 TEST 5 BAUD RATE ACCURACY

Before proceeding with this test the operator must install the RS 232C loopback jumper to connect (J35) at the back of the M20 Basic Module. See the end of this chapter for the loopback jumper configuration. The baud rate of the serial channels is set to 2400 baud, and 127 characters are transmitted. The time for the transmission is timed by the M20 motherboard 8253 and reports an error if the time is not within tolerance.

If this test is successful the message "Test complete. Enter any key to continue." appears.

6.6.7 TEST 6 INTERRUPT SUBSYSTEM

Before proceeding with this test the operator must connect the RS 232C loopback jumper to connector J35 at the back of the Basic Module. See the end of this section for the loopback jumper configuration.

Each of the interrupts are generated, and verified for isolation from other lines. During this phase of the test interrupts 0 through 3 are unmasked. This allows the program to identify interrupt lines shorted to one another.

Then all of the interrupts are generated with the interrupt controller inputs masked. The inputs to the interrupt controller are then unmasked and the proper order of the interrupt generation is verified. The test routines are such that errors are isolated to the interrupt sub-system or serial ports.

If the test is successful the message "Test complete. Enter any key to continue test." appears.

6.6.8 TEST & INTERRUPT DRIVEN DATA TRANSFER

Before proceeding with this test the operator must connect the RS 232C loopback jumper to connector (J35) at the back of the Basic Module. See the end of this section for the loopback jumper configuration.

A synchronous data transfer is performed, but in this case the transfer utilizes the interrupts. Data is transferred simultaneously in both directions. Errors are reported for data integrity, serial port status, and failure to synchronize.

If the test is successful the message "Test Complete. Enter any key to continue test." appears.

6.6.9 TEST 8 DEFAULT STRING

Before proceeding with this test the operator must connect an RS 232C loopback jumper to connector (J35) at the back of the Basic Module. See the end of this section for the loopback jumper configuration.

CURRENT LOOP

from pinto pin
 35.....20
 38.....19
 18.....37
 17.....40
 6.....3 (ground)
 23.....24(ground)
 13.....39
 34.....22
 7.....29 and 33
 8.....30 and 36
 28.....12 and 16
 25.....9 and 15

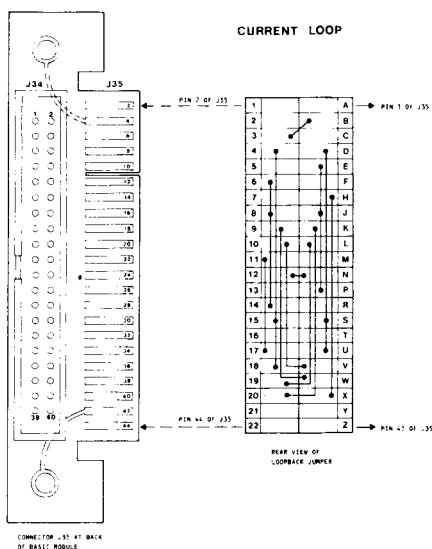


Fig. 6-9 Current Loop Loopback Jumper

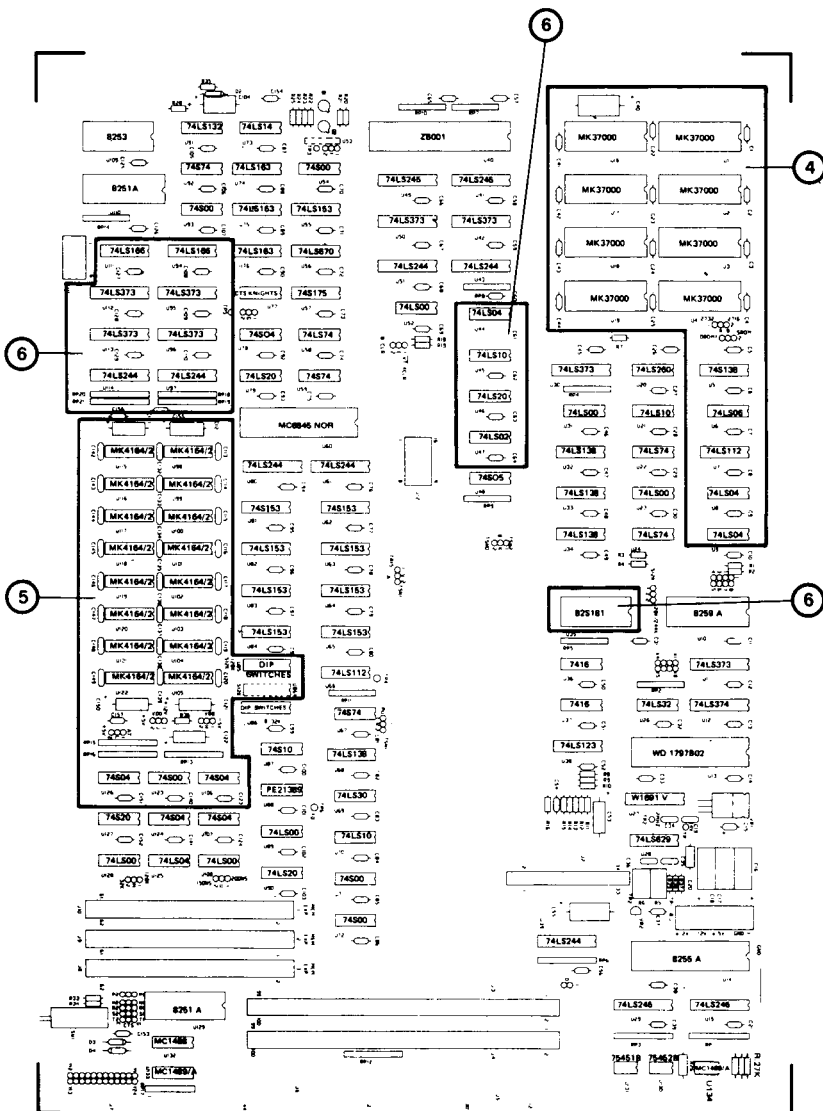
A. MOTHERBOARD CIRCUITRY

This appendix shows the principal M20 circuits' physical location on the motherboard.

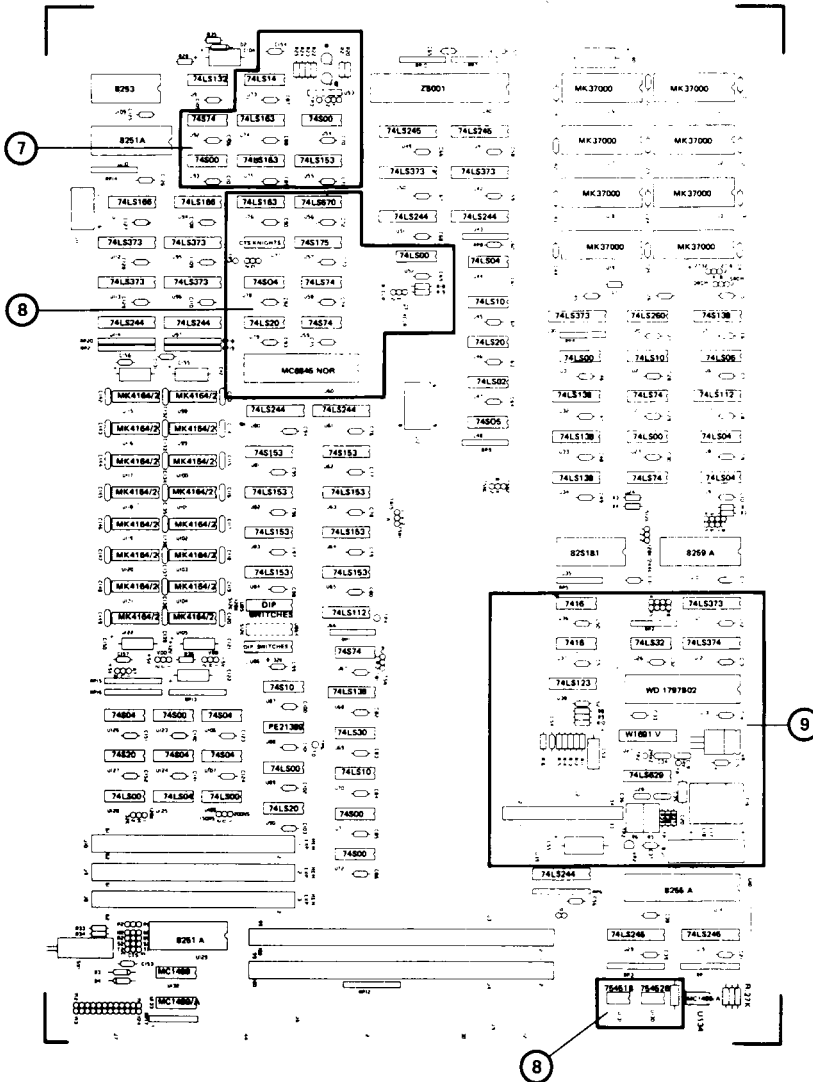
The motherboard is divided into the following 12 sections:

- 1 - CPU Circuit
- 2 - Memory Timing Circuitry
- 3 - Address Multiplexers
- 4 - Read Only Memory
- 5 - Random Access Memory
- 6 - Bit Map Circuitry
- 7 - Clock Circuitry
- 8 - Video Controller Circuitry
- 9 - Floppy Disk Controller
- 10- Timer and Parallel Interface
- 11- RS 232C Interface
- 12- Keyboard Interface

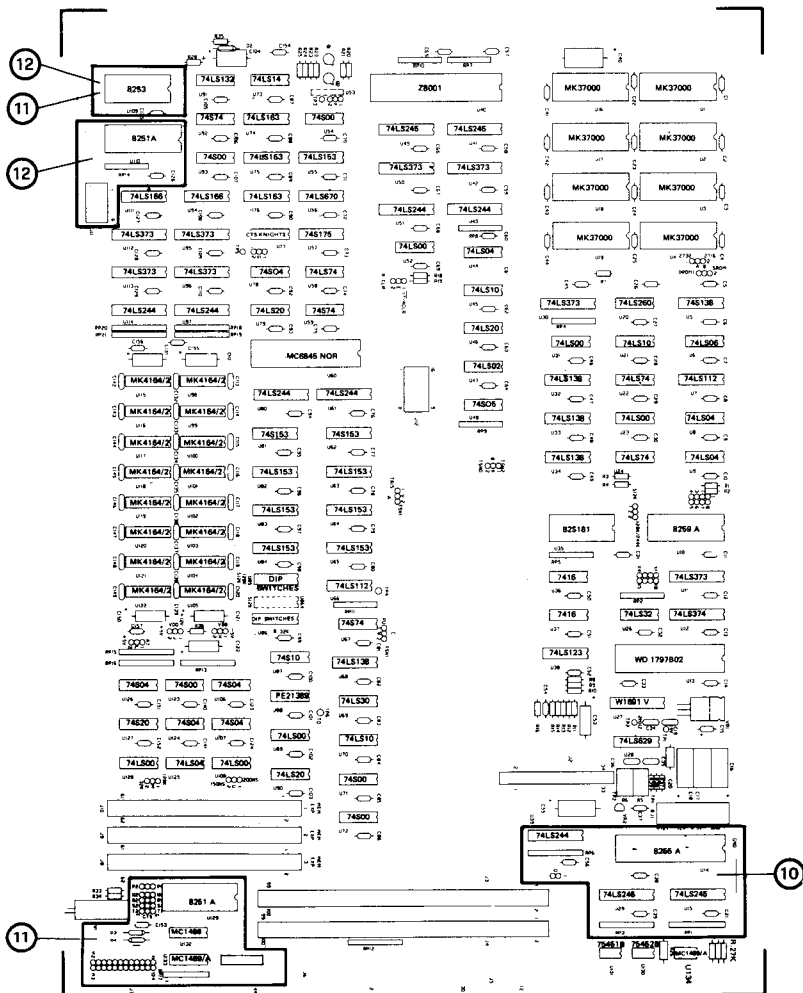
- 4) READ ONLY MEMORY
- 5) RAM
- 6) BIT MAP CIRCUIT



- 7) CLOCK CIRCUIT
- 8) VIDEO CONTROLLER
- 9) FLOPPY DISK CONTROLLER



- 10) TIMER AND PARALLEL INTERFACE
- 11) RS 232C INTERFACE
- 12) KEYBOARD INTERFACE



B. LIST OF DATC PUBLICATIONS

BIT		
Italian Code 3874272 S ! English Code 3874277 X		
No	TOPIC	DATE
01	Motherboard level CP1	4/82
02	Video Codes DSY 1036	4/82
03	Random problems on Display when in 'reverse' mode	5/82
04	Motherboard Level D3	5/82
05	Memory Map retrofitting	6/82
06	Motherboard Level D5 - Jumpers permanently soldered	8/82
07	Segment Violation Trap Problem on Z8001	8/82
08	Motherboard Changes for Colour Video DSY 1041/1046 Connection	10/82
09	ALI Board "LA12" Modification	10/82
10	Board "MI 181" Modification	10/82
11	LA12 Change of code to 126920 N	10/82
12	Board PWD-209 Modification	10/82
13	Preset for testing the Board G0 220 (IEEE 488) in the factory	10/82
14	Motherboard Level D7	1/83
15	Motherboard Level D9	1/83
16	Memory Expansion Boards (ME038, ME037 ME039, ME040)	12/82
17	Function Keys	12/82
18	Video Elcit Modifications	1/83

SOF		
Italian Code:3874294 V ! English Code: 3874299S		
No	TOPIC	DATE
01	System Test Release 1.05	5/82
02	Hard Disk Test Release 1.1	1/83
03	System Test Release 1.08	1/83

BIS		
Italian Code:3874284 V ! English Code: 3874289 Z		
No	TOPIC	DATE
01	Summary of PCOS rel 1.0 and 1.1	
02	Summary of PCOS release 1.3	11/82

NOP		
Italian Code:3874274 K ! English Code: 3874279 Q		
No	TOPIC	DATE
01	Colour Video DSY 1041	4/82
02	RS 232C Twin Jumper Configuration	10/82
03	Installation and Check of CPU 1049	12/82
04	Installation of APB 1086 Board	

LIS		
Italian Code:3874271 N ! English Code: 3874276 T		
No	TOPIC	DATE
01	Component List: Motherboard, Memory, Video B/W, Colour Video, IEEE 488	

C. SYSTEM TEST

CODE OF DISKETTE	SYSTEM TEST LEVEL	MOTHERBOARD LEVEL
H05170	1.06	up to D7
H05190	1.08	All levels

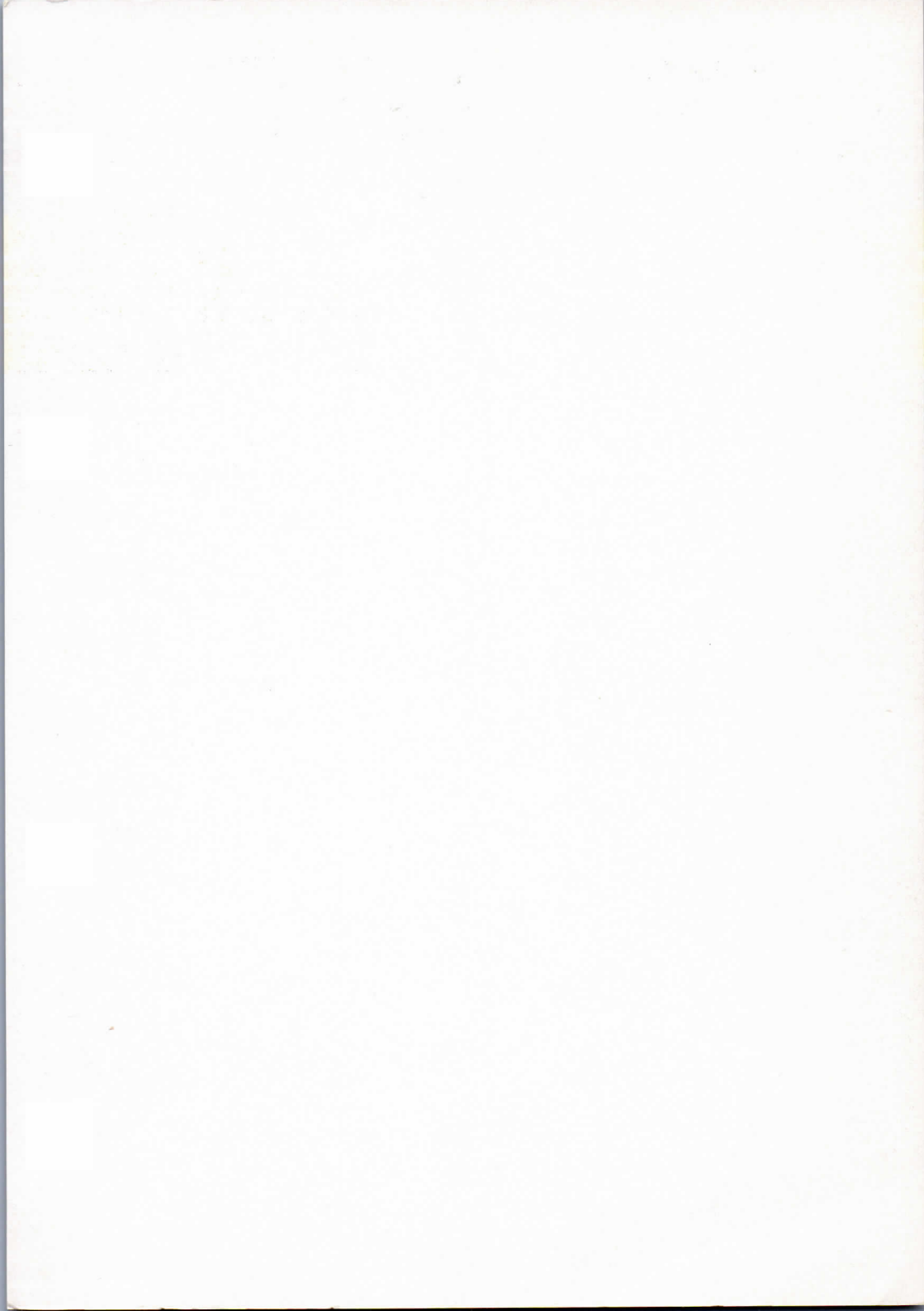
Code 4100380 V (0)

Printed in Italy

UPDATING STATUS

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Code 4100380 V (0)

Printed in Italy

PREDISPOSIZIONI SU PIASTRA INTERFACCIA IF002
Presetting on the Interface Board IF002

SELEZIONE OPZION
option Selection

	1307	
option	SA1	SA2
0P21.0ME	—	—
ALZAMASTRO COLORE SELECT.0M010 select colour ribbon 141E	OM	—
ALZAMASTRO COLORE DISSELE.0M010 Not select colour ribbon 141E	OFF	—
SWITCH TIME CARITA ABBLITATO End of paper enable switch	—	OM
SWITCH TIME CARITA DISABBLITATO End of paper disabled switch	—	OFF

FORMATO CARATTERE	
Character format	
811 B1 CODEC	STANDARD, SU TSD?
Code bit	Signal on TSD?
	DATA
7 011	0M
8 011	011
	0M

100

RELEASE	R0M1	R0M2	R0M3	R0M4	R0M5	R0M6	R0M7	R0M8	R0M9	R0M10	R0M11	R0M12	R0M13	R0M14	R0M15	R0M16	R0M17	R0M18	R0M19	R0M20	R0M21	R0M22	R0M23	R0M24	R0M25	R0M26	R0M27	R0M28	R0M29	R0M30	R0M31	R0M32	R0M33	R0M34	R0M35	R0M36	R0M37	R0M38	R0M39	R0M40	R0M41	R0M42	R0M43	R0M44	R0M45	R0M46	R0M47	R0M48	R0M49	R0M50	R0M51	R0M52	R0M53	R0M54	R0M55	R0M56	R0M57	R0M58	R0M59	R0M60	R0M61	R0M62	R0M63	R0M64	R0M65	R0M66	R0M67	R0M68	R0M69	R0M70	R0M71	R0M72	R0M73	R0M74	R0M75	R0M76	R0M77	R0M78	R0M79	R0M80	R0M81	R0M82	R0M83	R0M84	R0M85	R0M86	R0M87	R0M88	R0M89	R0M90	R0M91	R0M92	R0M93	R0M94	R0M95	R0M96	R0M97	R0M98	R0M99	R0M100	R0M101	R0M102	R0M103	R0M104	R0M105	R0M106	R0M107	R0M108	R0M109	R0M110	R0M111	R0M112	R0M113	R0M114	R0M115	R0M116	R0M117	R0M118	R0M119	R0M120	R0M121	R0M122	R0M123	R0M124	R0M125	R0M126	R0M127	R0M128	R0M129	R0M130	R0M131	R0M132	R0M133	R0M134	R0M135	R0M136	R0M137	R0M138	R0M139	R0M140	R0M141	R0M142	R0M143	R0M144	R0M145	R0M146	R0M147	R0M148	R0M149	R0M150	R0M151	R0M152	R0M153	R0M154	R0M155	R0M156	R0M157	R0M158	R0M159	R0M160	R0M161	R0M162	R0M163	R0M164	R0M165	R0M166	R0M167	R0M168	R0M169	R0M170	R0M171	R0M172	R0M173	R0M174	R0M175	R0M176	R0M177	R0M178	R0M179	R0M180	R0M181	R0M182	R0M183	R0M184	R0M185	R0M186	R0M187	R0M188	R0M189	R0M190	R0M191	R0M192	R0M193	R0M194	R0M195	R0M196	R0M197	R0M198	R0M199	R0M200	R0M201	R0M202	R0M203	R0M204	R0M205	R0M206	R0M207	R0M208	R0M209	R0M210	R0M211	R0M212	R0M213	R0M214	R0M215	R0M216	R0M217	R0M218	R0M219	R0M220	R0M221	R0M222	R0M223	R0M224	R0M225	R0M226	R0M227	R0M228	R0M229	R0M230	R0M231	R0M232	R0M233	R0M234	R0M235	R0M236	R0M237	R0M238	R0M239	R0M240	R0M241	R0M242	R0M243	R0M244	R0M245	R0M246	R0M247	R0M248	R0M249	R0M250	R0M251	R0M252	R0M253	R0M254	R0M255	R0M256	R0M257	R0M258	R0M259	R0M260	R0M261	R0M262	R0M263	R0M264	R0M265	R0M266	R0M267	R0M268	R0M269	R0M270	R0M271	R0M272	R0M273	R0M274	R0M275	R0M276	R0M277	R0M278	R0M279	R0M280	R0M281	R0M282	R0M283	R0M284	R0M285	R0M286	R0M287	R0M288	R0M289	R0M290	R0M291	R0M292	R0M293	R0M294	R0M295	R0M296	R0M297	R0M298	R0M299	R0M300	R0M301	R0M302	R0M303	R0M304	R0M305	R0M306	R0M307	R0M308	R0M309	R0M310	R0M311	R0M312	R0M313	R0M314	R0M315	R0M316	R0M317	R0M318	R0M319	R0M320	R0M321	R0M322	R0M323	R0M324	R0M325	R0M326	R0M327	R0M328	R0M329	R0M330	R0M331	R0M332	R0M333	R0M334	R0M335	R0M336	R0M337	R0M338	R0M339	R0M340	R0M341	R0M342	R0M343	R0M344	R0M345	R0M346	R0M347	R0M348	R0M349	R0M350	R0M351	R0M352	R0M353	R0M354	R0M355	R0M356	R0M357	R0M358	R0M359	R0M360	R0M361	R0M362	R0M363	R0M364	R0M365	R0M366	R0M367	R0M368	R0M369	R0M370	R0M371	R0M372	R0M373	R0M374	R0M375	R0M376	R0M377	R0M378	R0M379	R0M380	R0M381	R0M382	R0M383	R0M384	R0M385	R0M386	R0M387	R0M388	R0M389	R0M390	R0M391	R0M392	R0M393	R0M394	R0M395	R0M396	R0M397	R0M398	R0M399	R0M400	R0M401	R0M402	R0M403	R0M404	R0M405	R0M406	R0M407	R0M408	R0M409	R0M410	R0M411	R0M412	R0M413	R0M414	R0M415	R0M416	R0M417	R0M418	R0M419	R0M420	R0M421	R0M422	R0M423	R0M424	R0M425	R0M426	R0M427	R0M428	R0M429	R0M430	R0M431	R0M432	R0M433	R0M434	R0M435	R0M436	R0M437	R0M438	R0M439	R0M440	R0M441	R0M442	R0M443	R0M444	R0M445	R0M446	R0M447	R0M448	R0M449	R0M450	R0M451	R0M452	R0M453	R0M454	R0M455	R0M456	R0M457	R0M458	R0M459	R0M460	R0M461	R0M462	R0M463	R0M464	R0M465	R0M466	R0M467	R0M468	R0M469	R0M470	R0M471	R0M472	R0M473	R0M474	R0M475	R0M476	R0M477	R0M478	R0M479	R0M480	R0M481	R0M482	R0M483	R0M484	R0M485	R0M486	R0M487	R0M488	R0M489	R0M490	R0M491	R0M492	R0M493	R0M494	R0M495	R0M496	R0M497	R0M498	R0M499	R0M500	R0M501	R0M502	R0M503	R0M504	R0M505	R0M506	R0M507	R0M508	R0M509	R0M510	R0M511	R0M512	R0M513	R0M514	R0M515	R0M516	R0M517	R0M518	R0M519	R0M520	R0M521	R0M522	R0M523	R0M524	R0M525	R0M526	R0M527	R0M528	R0M529	R0M530	R0M531	R0M532	R0M533	R0M534	R0M535	R0M536	R0M537	R0M538	R0M539	R0M540	R0M541	R0M542	R0M543	R0M544	R0M545	R0M546	R0M547	R0M548	R0M549	R0M550	R0M551	R0M552	R0M553	R0M554	R0M555	R0M556	R0M557	R0M558	R0M559	R0M560	R0M561	R0M562	R0M563	R0M564	R0M565	R0M566	R0M567	R0M568	R0M569	R0M570	R0M571	R0M572	R0M573	R0M574	R0M575	R0M576	R0M577	R0M578	R0M579	R0M580	R0M581	R0M582	R0M583	R0M584	R0M585	R0M586	R0M587	R0M588	R0M589	R0M590	R0M591	R0M592	R0M593	R0M594	R0M595	R0M596	R0M597	R0M598	R0M599	R0M600	R0M601	R0M602	R0M603	R0M604	R0M605	R0M606	R0M607	R0M608	R0M609	R0M610	R0M611	R0M612	R0M613	R0M614	R0M615	R0M616	R0M617	R0M618	R0M619	R0M620	R0M621	R0M622	R0M623	R0M624	R0M625	R0M626	R0M627	R0M628	R0M629	R0M630	R0M631	R0M632	R0M633	R0M634	R0M635	R0M636	R0M637	R0M638	R0M639	R0M640	R0M641	R0M642	R0M643	R0M644	R0M645	R0M646	R0M647	R0M648	R0M649	R0M650	R0M651	R0M652	R0M653	R0M654	R0M655	R0M656	R0M657	R0M658	R0M659	R0M660	R0M661	R0M662	R0M663	R0M664	R0M665	R0M666	R0M667	R0M668	R0M669	R0M670	R0M671	R0M672	R0M673	R0M674	R0M675	R0M676	R0M677	R0M678	R0M679	R0M680	R0M681	R0M682	R0M683	R0M684	R0M685	R0M686	R0M687	R0M688	R0M689	R0M690	R0M691	R0M692	R0M693	R0M694	R0M695	R0M696	R0M697	R0M698	R0M699	R0M700	R0M701	R0M702	R0M703	R0M704	R0M705	R0M706	R0M707	R0M708	R0M709	R0M710	R0M711	R0M712	R0M713	R0M714	R0M715	R0M716	R0M717	R0M718	R0M719	R0M720	R0M721	R0M722	R0M723	R0M724	R0M725	R0M726	R0M727	R0M728	R0M729	R0M730	R0M731	R0M732	R0M733	R0M734	R0M735	R0M736	R0M737	R0M738	R0M739	R0M740	R0M741	R0M742	R0M743	R0M744	R0M745	R0M746	R0M747	R0M748	R0M749	R0M750	R0M751	R0M752	R0M753	R0M754	R0M755	R0M756	R0M757	R0M758	R0M759	R0M760	R0M761	R0M762	R0M763	R0M764	R0M765	R0M766	R0M767	R0M768	R0M769	R0M770	R0M771	R0M772	R0M773	R0M774	R0M775	R0M776	R0M777	R0M778	R0M779	R0M780	R0M781	R0M782	R0M783	R0M784	R0M785	R0M786	R0M787	R0M788	R0M789	R0M790	R0M791	R0M792	R0M793	R0M794	R0M795	R0M796	R0M797	R0M798	R0M799	R0M800	R0M801	R0M802	R0M803	R0M804	R0M805	R0M806	R0M807	R0M808	R0M809	R0M810	R0M811	R0M812	R0M813	R0M814	R0M815	R0M816	R0M817	R0M818	R0M819	R0M820	R0M821	R0M822	R0M823	R0M824	R0M825	R0M826	R0M827	R0M828	R0M829	R0M830	R0M831	R0M832	R0M833	R0M834	R0M835	R0M836	R0M837	R0M838	R0M839	R0M840	R0M841	R0M842	R0M843	R0M844	R0M845	R0M846	R0M847	R0M848	R0M849	R0M850	R0M851	R0M852	R0M853	R0M854	R0M855	R0M856	R0M857	R0M858	R0M859	R0M860	R0M861	R0M862	R0M863	R0M864	R0M865	R0M866	R0M867	R0M868	R0M869	R0M870	R0M871	R0M872	R0M873	R0M874	R0M875	R0M876	R0M877	R0M878	R0M879	R0M880	R0M881	R0M882	R0M883	R0M884	R0M885	R0M886	R0M887	R0M888	R0M889	R0M890	R0M891	R0M892	R0M893	R0M894	R0M895	R0M896	R0M897	R0M898	R0M899	R0M900	R0M901	R0M902	R0M903	R0M904	R0M905	R0M906	R0M907	R0M908	R0M909	R0M910	R0M911	R0M912	R0M913	R0M914	R0M915	R0M916	R0M917	R0M918	R0M919	R0M920	R0M921	R0M922	R0M923	R0M924	R0M925	R0M926	R0M927	R0M928	R0M929	R0M930	R0M931	R0M932	R0M933	R0M934	R0M935	R0M936	R0M937	R0M938	R0M939	R0M940	R0M941	R0M942	R0M943	R0M944	R0M945	R0M946	R0M947	R0M948	R0M949	R0M950	R0M951	R0M952	R0M953	R0M954	R0M955	R0M956	R0M957	R0M958	R0M959	R0M960	R0M961	R0M962	R0M963	R0M964	R0M965	R0M966	R0M967	R0M968	R0M969	R0M970	R0M971	R0M972	R0M973	R0M974	R0M975	R0M976	R0M977	R0M978	R0M979	R0M980	R0M981	R0M982	R0M983	R0M984	R0M985	R0M986	R0M987	R0M988	R0M989	R0M990	R0M991	R0M992	R0M993	R0M994	R0M995	R0M996	R0M997	R0M998	R0M999	R0M1000	R0M1001	R0M1002	R0M1003	R0M1004	R0M1005	R0M1006	R0M1007	R0M1008	R0M1009	R0M1010	R0M1011	R0M1012	R0M1013	R0M1014	R0M1015	R0M1016	R0M1017	R0M1018	R0M1019	R0M1020	R0M1021	R0M1022	R0M1023	R0M1024	R0M1025	R0M1026	R0M1027	R0M1028	R0M1029	R0M1030	R0M1031	R0M1032	R0M1033	R0M1034	R0M1035	R0M1036	R0M1037	R0M1038	R0M1039	R0M1040	R0M1041	R0M1042	R0M1043	R0M1044	R0M1045	R0M1046	R0M1047	R0M1048	R0M1049	R0M1050	R0M1051	R0M1052	R0M1053	R0M1054	R0M1055	R0M1056	R0M1057	R0M1058	R0M1059	R0M1060	R0M1061	R0M1062	R0M1063	R0M1064	R0M1065	R0M1066	R0M1067	R0M1068	R0M1069	R0M1070	R0M1071	R0M1072	R0M1073	R0M1074	R0M1075	R0M1076	R0M1077	R0M1078	R0M1079	R0M1080	R0M1081	R0M1082	R0M1083	R0M1084	R0M1085	R0M1086	R0M1087	R0M1088	R0M1089	R0M1090	R0M1091	R0M1092	R0M1093	R0M1094	R0M1095	R0M1096	R0M1097	R0M1098	R0M1099	R0M1100	R0M1101	R0M1102	R0M1103	R0M1104	R0M1105	R0M1106	R0M1107	R0M1108	R0M1109	R0M1110	R0M1111	R0M1112	R0M1113	R0M1114	R0M1115	R0M1116	R0M1117	R0M1118	R0M1119	R0M1120	R0M1121	R0M1122	R0M1123	R0M1124	R0M1125	R0M1126	R0M1127	R0M1128	R0M1129	R0M1130	R0M1131	R0M1132	R0M1133	R0M1134	R0M1135	R0M1136	R0M1137	R0M1138	R0M1139	R0M1140	R0M1141	R0M1142	R0M1143	R0M1144	R0M1145	R0M1146	R0M1147	R0M1148	R0M1149	R0M1150	R0M1151	R0M1152	R0M1153	R0M1154	R0M1155	R0M1156	R0M1157	R0M1158	R0M1159	R0M1160	R0M1161	R0M1162	R0M1163	R0M1164	R0M1165	R0M1166	R0M1167	R0M1168	R0M1169	R0M1170	R0M1171	R0M1172	R0M1173	R0M1174	R0M1175	R0M1176	R0M1177	R0M1178	R0M1179	R0M1180	R0M1181	R0M1182	R0M1183	R0M1184	R0M1185	R0M1186	R0M1187	R0M1188	R0M1189	R0M1190	R0M1191	R0M1192	R0M1193	R0M1194	R0M1195	R0M1196	R0M1197	R0M1198	R0M1199	R0M1200	R0M1201	R0M1202	R0M1203	R0M1204	R0M1205	R0M1206	R0M1207	R0M1208	R0M1209	R0M1210	R0M1211	R0M1212	R0M1213	R0M1214	R0M1215	R0M1216	R0M1217	R0M1218	R0M1219	R0M1220	R0M1221	R0M1222	R0M1223	R0M1224	R0M1225	R0M12
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[illegible]

TIPO INTERFACCIA	
Interface Type	
	TS08-Sw4
CENTRONICS	ON
DATA PRODUCTS	OFF

OFF

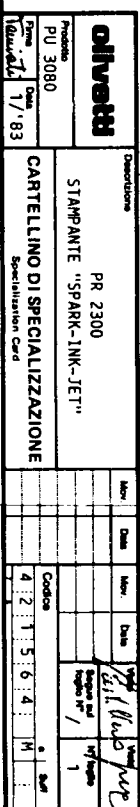
— NON SIGNIFICATIVO / Not significant

Modelo
XU 7320

	Mov.	Data	Mov.	Data	Visto <i>[Signature]</i>	Visto
					Sigla sul loggio N° 212	N° loggio 112
Codice						
a						Swit.

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2.7.3.6 PR 430 Jumper Settings

Il presente cartellino deve essere compilato dal tecnico STAC all'atto dell'installazione. (Apporre una X in corrispondenza della configurazione scelta).
This card should be completed by the STAC technician during installation. (Enter "X" next to configuration chosen).

INTENSITA' DI BATTUTA STROKE IMPACT

1	2	3	4	5	6
16	15	14	13	12	11

TIPO INTERLINEA TYPE OF LINE FEED

NORMALE - STANDARD	
RUYS - RUYS	
ZURIGO - ZURIGO	

ROM MICROPROGRAMMI ROM MICROPROGRAMS

PRESENZA OPZIONI OPTIONAL EXTRAS PRESENT

SPROCKET SF 436	4	6
METTIFOGGIO ASF 435	4	7
AUTOMATIC SHEET FEED ASF 435		

GENERATORI CARATTERI MBAC-MBAX/WP CHARACTER GENERATION MBAC-MBAX/WP

CRT	MBAC	NAZIONE COUNTRY	J054 (G0092)
200	160	ITALIA ITALY	4 32 33 40
201	161	FRANCIA FRANCE	4 33 40
206	166	INGHILTERRA GREAT BRITAIN	4 40
204	164	USA - AUSTRALIA USA and AUSTRALIA	4 30
202	162	OLANDA HOLLAND	---
205	165	CANADA FR. FRENCH-SPEAKING	4 32
203	163	GERMANIA AUSTRIA GERMANY and AUSTRIA	4 32 40
207	167	DANIMARCA DENMARK	4 32 33

GENERATORI CARATTERI MBAD-EDP CHARACTER GENERATION MBAD-EDP

CRT	NAZIONE COUNTRY	J054 (G0092)
122	ITALIA ITALY	4 32 33 40
117	FRANCIA FRANCE	4 33 40
123	INGHILTERRA GREAT BRITAIN	4 40
116	USA - ASCII USA - ASCII	4 33
118	SPAGNA SPAIN	---
124	SVIZZERA SWITZERLAND	4 32
121	GERMANIA GERMANY	4 32 40
115	PORTOGALLO - PORTUGAL and BRAZIL	4 32 33

GENERATORI CARATTERI MBAX/WP CHARACTER GENERATION MBAX/WP

CRT	NAZIONE COUNTRY	J054 (G0092)
210	SVIZZERA FRANC WP SWITZERLAND FRENCH-SPEAKING	4 32 33 40
211	SVIZZERA TEDESCA WP SWITZERLAND GERMAN-SPEAKING	4 33 40
212	FINLANDIA WP FINLAND	4 32 40
208	SUD AFRICA WP SOUTH AFRICA	4 40
214	GIAPPONE JAPAN	4 32
209	MESSICO WP MEXICO	4 33
213	YUGOSLAVIA YUGOSLAVIA	4 32 33
215	SPAGNA WP SPAIN	---

GENERATORI CARATTERI PAEA-WP EDP CHARACTER GENERATION PAEA-WP EDP

CRT	NAZIONE COUNTRY	J054 (G0092)
173	SVIZZERA FRANC WP SWITZERLAND FRENCH-SPEAKING	4 32 33 40
172	SVIZZERA TEDESCA WP SWITZERLAND GERMAN-SPEAKING	4 33 40
175	FINLANDIA WP FINLAND	4 32 40
171	SUD AFRICA WP SOUTH AFRICA	4 40
119	DANIMARCA EDP DENMARK	4 32 33
170	MESSICO WP MEXICO	4 33
120	SVEZIA - FINL EDP SWEDEN - FINLAND	4 32
174	SPAGNA WP SPAIN	---

Prontimmarzione grafica - General programming

MODI DI FUNZIONAMENTO OPERATING MODE

TEST STAC STAC TEST		J054 (G0092)
FREE RUNNING	4 17	
FULL-DUPLEX - PROCEDURA DI COLLOQUIO FULL-DUPLEX PROCEDURE	4 18	
XON - XOFF (FREE RUNNING)	4 18 19	

VARIANTI PRESTAZIONALI OPERATIONAL VARIANTS

INVIO BREAK ALL ACCEN SIONE (240 msec.) BREAK GENERATION UPON SWITCH-ON (240 msec.)	4 20	J054 (G0092)
TEST CONTINUO (VRP 40) CONTINUOUS TEST (VRP 40)	4 21	
FORZA CR DOPO MOVIMENTO CARTA (VRP 50) CARRIAGE RETURN AFTER LINE FEED (VRP 50)	4 22	
PONI LOCALE PER BELL (VRP 60) LOCAL SETTING FOR BELL (VRP 60)	4 23	
FORZA LF DOPO CR (NAZ40) LINE FEED AFTER CARRIAGE RETURN	4 41	

FORMATO CARATTERE CHARACTER FORMAT

7 bit	4 8	J054 (G0092)
8 bit		
PARITÀ PARI EVEN PARITY		
PARITÀ DISPARI ODD PARITY	4 10	
SENZA PARITÀ WITHOUT PARITY	4 9	
1 STOP STOP	4 12	
1.5 bit di STOP 1.5 STOP bits	4 11	
2 bit di STOP 2 STOP bits		

VELOCITÀ SCAMBIO DATI DATA EXCHANGE SPEED

110 B/s		J054 (G0092)
110 bits per second		
134.5 B/s	4 13 15 16	
150 B/s	4 16	
200 B/s	4 13 15	
300 B/s	4 15	
600 B/s	4 13 16	
1200 B/s	4 14	
1800 B/s	4 14 16	
2400 B/s	4 15 16	
4800 B/s	4 14 15	
9600 B/s	4 14 15 16	

TENSIONE RETE MAINS VOLTAGE

100V - 60 Hz	1 3 4 - 8 2 7
115V - 60 Hz	1 5 6 - 9 2 7
220V - 60 Hz	1 9 6 7

TENSIONE RETE MAINS VOLTAGE

100V - 50 Hz	1 3 4 - 8 2 7
120V - 50 Hz	1 5 6 - 9 2 7
200V - 50 Hz	1 8 4 7
220V - 50 Hz	1 8 6 7
240V - 50 Hz	1 9 6 7

Selezionare PR430 (CON ALI 254)

PIASTRE : AT633 - G0092 - F063

Prodotto XU7750

Data 10-12-80

2-14

PRINTED IN ITALY BY OLIVETTI METODI - VIREA

4100380 V

Programmazione specifica per EIARS 232/C Specific programming for EIARS 232/C

MODALITA' SCAMBIO DATI DATA EXCHANGE PROCEDURES	J054 (G0092)
--	-----------------

FULL DUPLEX - PROCEDURA DI COLLOQUIO	4 - 18
FULL-DUPLEX - PROCEDURE	38 - 29
	34 - 36

XON · XOFF (FREE RUNNING)

N.B.: Scollegare il ponticello 34 - 35 su J054
Disconnect jumper 34 - 35 on J054.

MODALITA' SCAMBIO DATI DATA EXCHANGE PROCEDURES	J054 (G0092)
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PROCEDURA FULL-DUPLEX	4 . 18
FULL-DUPLEX PROCEDURE	26 . 27
	29 . 30
	37 . 38

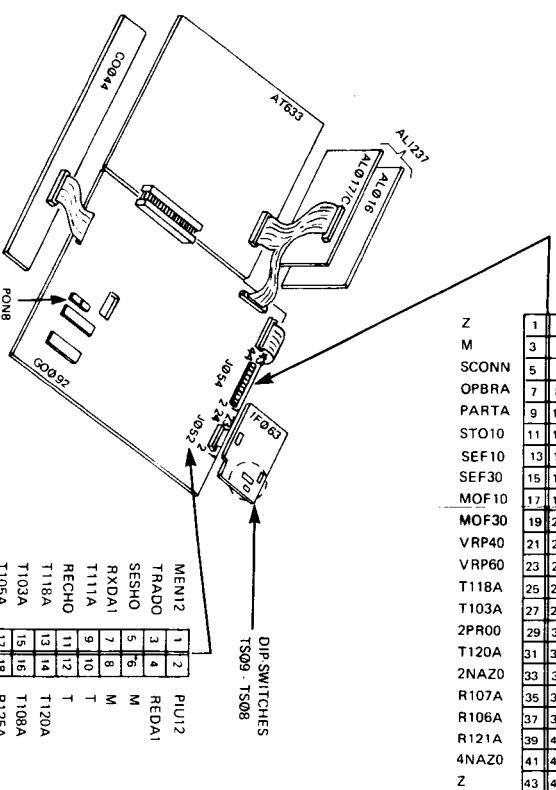
FREE RUNNING CON OCCUPATO	4. 17
SU TRANSMITTED DATA (BREAK)	26. 27
FREE RUNNING WITH BUSY SIGNAL	29. 30
FOR TRANSMITTED DATA (BREAK)	37. 38

FREE RUNNING CON OCCUPATO	4. 18. 19
SU TX DATA (DC1 - DC3)	26. 27
FREE RUNNING WITH BUSY SIGNAL	29. 30
FOR TX DATA (DC1 - DC3)	37. 38

FREE RUNNING CON OCCUPATO SU SECONDARY TRANSMITTED DATA	4. 17 29. 31 38. 39
FREE RUNNING WITH BUSY SIGNAL	

FOR SECONDARY TRANSMITTED DATA	28
FREE RUNNING CON OCCUPATO SU REVERSE CHANNEL FREE RUNNING WITH BUSY SIGNAL FOR REVERSE CHANNEL	4 . 17 26 . 28 29 . 30 38

	TS69		TS68	
	1	2	3	4
● DIP SWITCHES ON				
TX ATTIVO 20 mA ACTIVE TX 20 mA	●	●	●	
TX ATTIVO 60 mA ACTIVE TX 60 mA	●	●	●	
TX PASSIVO PASSIVE TX	●	●		
RX ATTIVO 20 mA ACTIVE RX 20 mA		●	●	●
RX ATTIVO 60 mA ACTIVE RX 60 mA		●	●	●
RX PASSIVO PASSIVE RX		●	●	



MASSA LOGICĂ (PUNTI 4 . 3 . 44)

DATO L'ESIGUO NUMERO DEI PUNTI DI MASSA, SI CONSIGLIA DI RAGGRUPPARE TRA LORO (A FESTEONE) PIU' SEGNALI DA COLLEGARE A MASSA.

*** LOGIC EARTH (PINS 4 - 3 - 44).
IN VIEW OF THE SMALL NUMBER OF EARTH PINS
THE SIGNALS WHICH ARE TO BE EARTHED SHOULD
BE DAISY CHAIN CONNECTED.**

N° foglio 2/2	Codice	
	■	Sub
	6 6 5 8 8 2 Z	x x x

2.7.4 CONNECTING TO AN AC SOURCE

The power switch on the Basic Module as well as the power switch on the printer should be off. The AC mains cable exits from the rear of the Basic Module. This cable should be connected to an appropriate power outlet, AFTER HAVING VERIFIED THAT THE VOLTAGE INDICATED ON THE STICKER AT THE REAR OF THE BASIC MODULE INDICATES THE SAME VOLTAGE AS THE POWER OUTLET TO BE USED. Two wire extensions should not be used.

2.7.5 SWITCHING ON (CPU 1042)

Insert the system diskette in one of the disk drives. The power switch on the Basic Module can now be switched on. The Light Emitting Diode (LED) on the keyboard should light up. If the LED does not light one has to immediately check the power outlet. If the LED is on, after about 8 seconds the following should appear on the display:

```
-----  
M20 system configuration:  
total memory size:   XXX kbytes  
user memory size:   XXX kbytes  
display tpe:        Black and White or Color  
disk drive(s):      X ready  
L1.M20 PCOS VER. XX  
-----
```

This means that the Power Up diagnostics have run successfully. Power up diagnostics which are run automatically after switching on or after pushing the RESET button verify that enough of the M20 functions are operable to allow the running of additional diagnostic programs. If the power up diagnostics do not run to completion an error code should appear on the Display and on the printer. Refer to the power Up diagnostics chapter for a detailed account of these diagnostics.

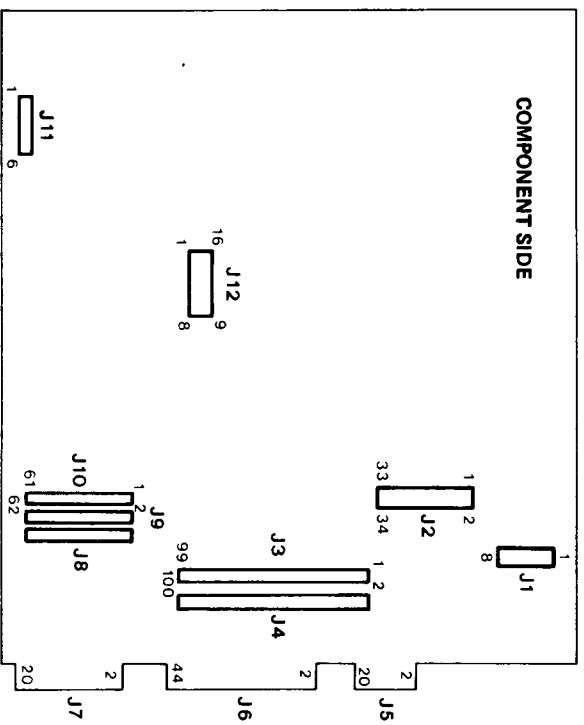
Turning the printer on and off while the computer is in use may cause abnormal operation and the computer may 'hang up', requiring the user to reset the system. It should be pointed out to the customer that he should not switch on and off the system unnecessarily. Should something go wrong during the operation of the system, the user should first press the Control key in conjunction with the RESET key on the keyboard. If this operation has no effect the RESET button located at the right rear side of the Basic Module should be pressed.

2.7.5.1 Procedures To Be Followed When Installing Hard Disk Systems

This section describes the procedure for installing PCOS on a hard disk M20 system. This section covers both the first installation and also updating the hard disk drive with a new version of PCOS.

2.10 CONNECTOR DESCRIPTIONS

This section shows all the connectors used on the M20 motherboard.



- J1 POWER CONNECTOR
- J2 FLOPPY DISK DRIVE CONNECTOR
- J3 } BUS CONNECTOR (IEEE, VIDEOTEX, TWIN RS 232 C, APB 1086)
- J4 }
- J5 VIDEO CONNECTOR
- J6 PARALLEL INTERFACE CONNECTOR
- J7 SERIAL INTERFACE CONNECTOR (RS 232 C)
- J8 MEMORY EXPANSION BOARD CONNECTOR
- J9 MEMORY EXPANSION BOARD CONNECTOR
- J10 MEMORY EXPANSION BOARD CONNECTOR
- J11 KEYBOARD CONNECTOR
- J12 VIDEOTEX CONNECTOR

